YAMAHA

YGV638

VC2

Video Controller 2

■ Overview

· YGV638 (also called “VC2”) is a pattern graphic controller with an on-chip VRAM and the ample drawing performance enables high-resolution animated GUIs on WVGA display panels.

· YGV638’s multiple video ports allow direct handling of video signals from various sources: DVD players, car navigation systems, rear view cameras, etc.
In addition, YGV638 is capable of superimposing characters, lines, and even graphic icons or menu screens (hereinafter called “sprite”) onto these videos.

· With conventional graphic controllers, complicated display control programs need to be developed. With YGV638, Sprites can be used to simplify the programs as all the controls of a Sprite is available in its 12-byte attribute: position, scaling factor, transparency, color gradation, etc.

· YGV638 integrates image de-compression engine (Yamaha proprietary algorithm) to dynamically decompress the Sprite data stored in its external memory (Flash ROM etc.) achieving substantial memory capacity savings.

YGV638, with the features above, allows display systems for in-vehicle AV equipments, audio equipments with display to be built with low-cost components.

YAMAHA CORPORATION

YGV638 CATALOG
CATALOG No. LSI-4GV638A22
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■ Features

■ Display Function

- Video Output
  - · Monitor supported: TFT liquid crystal display (digital RGB connection) or compatible display equipments
  - · Digital RGB666, Digital RGB666+FRC, Digital RGB888
  - · Supports NTSC, PAL, QVGA, WQVGA, VGA, WVGA, and SVGA
  - · Supports interlace and progressive scans
  - · Supports display timings in 1 dot and in 1 line resolution
  - · Equalizing pulse insertion for composite sync signals
  - · Dot clock polarity selection
  - · Sync signal polarity selection
  - · Gamma correction function (look-up table based)
  - · On-chip LCD timing controller
- Display Plane Functions
  - · Up to 341 planes (up to 128 planes per scan line) and one external video plane
  - · A layer displays either sprites, lines or texts
  - · Alpha-blending between layers
  - · Alpha-blending between layer and external video
  - · Picture attribute controls by layers (contrasts, brightness)

■ Layer Function

- Sprite
  - · Displaying up to 341 sprites per screen and up to 128 sprites per scan line
  - · Specified by horizontal and vertical coordinates
  - · Sizes from 8 dot × 8 dot to 1024 dot × 1024 dot. Horizontal and vertical scaling independently selectable (in 8-dot unit)
  - · 2, 16, 64, or 256 palette colors from 16M colors, or 64K colors with 16-bit RGB, 256K colors with 18-bit RGB, and 16M colors, life-like picture quality with 24-bit RGB
  - · Scaling Function
  - · Anti-aliasing of the outline profile
  - · On-chip palettes with 1024 colors (combinations of 2 color palettes, 16 color palettes, 64 color palettes, and 256 color palettes up to 1024 colors in total)

- Text
  - Displaying up to 1948 characters per screen and up to 128 characters per scan line
  - Independent font selections for each character strings
  - Supports proportional font
  - Supports half-width font
  - Scaling function
  - Supports 4-bit/pixel anti-aliasing font
  - Font size: 1 dot × 1 dot to 64 dot × 64 dot in increments of 1-dot independently in horizontal and vertical direction
- Line
  - Line drawn directly from specifications of start/end point coordinates
  - Up to 510 lines per screen
  - 32768-color (RGB555) specification or palette index (10 bits) specification
  - Line width: from 1 dot to 16 dots (in one dot increments)
  - Anti-aliasing drawing function

■ Video Signal Inputs

- Analog Video Input
  - Compatible with composite video, S video, component video, and RGB signal inputs
  - On-chip three 10bit-ADCs
  - Compatible with NTSC and PAL signal formats
  - On-chip video decoder
  - Supports interlace and progressive scans (RGB)
  - Compatible with composite sync signal inputs (RGB)
- Digital Video Input
  - Compatible with RGB666, 16bit YCrCb, and 8bit YCrCb (ITU-R BT.656)
  - Compatible with interlace and progressive scans
  - Compatible with composite sync signal inputs
- Video Image Processing
  - Scaling (the input images scaled to fit the display resolution, not a zooming function)
  - Mirror flipping (through vertical axis)
  - External sync mode (or free-running mode: switchable)

■ Video Decoder

- On-chip High-quality Y/C Separation Circuit (2D adaptive comb filter)
- Digital AGC Circuit
- Image Color Controls
  - Contrast
  - Brightness
  - Color hue
  - Chroma saturation
- Color Killer Function

■ Other Features

- CPU Interface
  - Serial or 8-bit parallel connection
  - Indirect accesses to internal registers and tables through single access port
  - Flexible asynchronous bus interface
  - Macro command function
- Pattern Memory Interface
  - Bus width of 32 bits, or 16 bits
  - Up to 512 Mbits (64 MB) memory
  - Supports Mask-ROM, NOR-type flash-memory, SRAM, or compatible timing memories
  - Supports Page Mode accesses
  - Access timings in multiples of the system clock cycle
- Device Specifications
  - Lead-free 208-pin LQFP package (YGV638-VZ)
  - Supply voltages: 3.3V and 1.8V
  - CPU interface power supply 3.3V
  - Operating temperature range from -40℃ to +85℃

■ Pin Attributes

Pin Name	Num.	I/O	Function	Attribute	Drive
CPU Interface (22)					
D7-0	8	I/O	CPU data bus	Tolerant	4mA
PS2-0	3	I	CPU port selection	Tolerant	
CS_N	1	I	Chip select (dual-purpose pin)	Tolerant	
RD_N	1	I	Read strobe (dual-purpose pin)	Tolerant	
WR_N	1	I	Write strobe (dual-purpose pin)	Tolerant	
WAIT_N	1	OT	CPU bus wait (dual-purpose pin)	Tolerant	4mA
READY_N	1	OT	CPU bus ready	Tolerant	4mA
INT_N	1	OD	Interrupt	Tolerant	4mA
SER_N	1	I	CPU interface selection		
SCS_N	1	I	Serial interface chip select (dual-purpose pin)	Tolerant	
SDIN	1	I	Serial interface data input (dual-purpose pin)	Tolerant	
SCLK	1	I	Serial interface clocked into (dual-purpose pin)	Tolerant	
SDOUT	1	OT	Serial interface data output (dual-purpose pin)	Tolerant	4mA
Pattern Memory Interface (60)					
MD31-0	32	I/O	Pattern memory data bus		4mA
MA25-1	25	OT	Pattern memory address bus		4mA
MOE_N	1	OT	Pattern memory output enable		4mA
MWE_N	1	OT	Pattern memory write pulse		4mA
RAHZ_N	1	I	Pattern memory high-impedance switching pin	Tolerant	
Video Input (58)					
ACIN1	1	I	Analog composite video input	Analog	
ACIN2	1	I	Analog composite video input	Analog	
ARIN	1	I	Analog video R input	Analog	
AGIN	1	I	Analog video G input	Analog	
ABIN	1	I	Analog video B input	Analog	
ATESTIN	1	I	Test input	Analog	
VREF0	1	O	ADC reference	Analog	
VREFP	1	O	Plus reference voltage for ADC	Analog	
VREFN	1	O	Minus reference voltage for ADC	Analog	
ADCKIN	1	I	Analog video clock input	Tolerant	
ARCKIN	1	I	Analog video clock input	Tolerant	
AVSIN_N	1	I	Analog video vertical sync signal input	Tolerant	
AHSIN_N	1	I	Analog video horizontal sync signal input	Tolerant	
DRI7-2	6	I	Digital video R input (dual-purpose pin)	Tolerant	
DGI7-2	6	I	Digital video G input (dual-purpose pin)	Tolerant	
DBI7-2	6	I	Digital video B input (dual-purpose pin)	Tolerant	
DIN7-0	8	I	Digital video 8bit YCrCb input (dual-purpose pin)	Tolerant	
YIN7-0	8	I	Digital video Y input (dual-purpose pin)	Tolerant	
CIN7-0	8	I	Digital video Cr/Cb input (dual-purpose pin)	Tolerant	
DVSIN_N	1	I	Digital video vertical sync signal input	Tolerant	
DHSIN_N	1	I	Digital video horizontal sync signal input	Tolerant	
DGCKIN	1	I	Digital video clock input	Tolerant	

Monitor Interface (34)					
DRO7-0	8	O	Digital video: R output		4mA
DGO7-0	8	O	Digital video: G output		4mA
DBO7-0	8	O	Digital video: B output		4mA
VSYNC_N	1	OT	Vertical sync signal output (dual-purpose pin)	Tolerant	4mA
HCSYNC_N	1	OT	Horizontal sync signal or composite sync signal output (dual-purpose pin)	Tolerant	4mA
BLANK_N	1	OT	Display timing output (dual-purpose pin)	Tolerant	4mA
STARTH	1	OT	Horizontal start signal output	Tolerant	4mA
LOADH	1	OT	Horizontal load signal output	Tolerant	4mA
CLKV	1	OT	Vertical clock output (dual-purpose pin)	Tolerant	4mA
STARTV	1	OT	Vertical start signal output (dual-purpose pin)	Tolerant	4mA
POL	1	OT	Polarity reverse output (dual-purpose pin)	Tolerant	4mA
OUTENV	1	OT	Output enable signal for a gate driver output	Tolerant	4mA
DOTCLK	1	O	Dot clock output		4mA
Clock & Reset (8)					
XIN	1	I	Reference clock input		
XOUT	1	O	Crystal connection		
DTCKIN	1	I	Dot clock input	Tolerant	
PLLCTL3-0	4	I	PLL control		
RESET_N	1	I$	Reset	Tolerant	
for device (56)					
XTEST2-0	3	I	Test pin		
VDD33	17	—	Digital I/O power supply		
VSS	19	—	Digital I/O VSS		
PLLVDD	1	—	Power supply for system clock generation PLL		
PLLVSS	1	—	VSS for system clock generation PLL		
APLLVDD	1	—	Power supply for analog RGB clock generation PLL		
APLLVSS	1	—	VSS for analog RGB clock generation PLL		
AVDD33	1	—	Power supply for Analog Front End		
AVDD18	2	—	Power supply for Analog Front End		
AVSS	2	—	VSS for Analog Front End		
VDD18	4	—	Power supply for digital core		
VSS18	4	—	VSS for digital core		
others (1)					
NC	1	—	No connection pin		

Total number of pins: 239 pin - 31 dual-purpose pin = 208 pins

[Description of I/O]

I:	Input	I$:	Input with Schmitt trigger	I/O:	Input and Output
O:	Output	OT:	3-state output	OD:	Open-drain output

[Description of attribute]

Tolerant: An attribute of an input pin buffer and a bidirectional pin buffer, or the output pin buffer. During high impedance states, current will not flow into power supply pins from a pin when some voltage higher than the I/O supply voltage is applied to the pin, if the pin is "Tolerant."

Analog: Attribute which indicates an analog pin. These pins are operated from AVDD33 power supply.

· Sharing Pins

On YGV638,

- the CPU interface pins change functions depending on which CPU interface, parallel or serial, is used.
- the digital video input pins change functions depending on the digital video input format used.
- the monitor interface pins change functions when the integrated LCD timing controller is used.

i) Sharing of CPU Interface Pins

YGV638 supports the 8-bit parallel interface or serial interface. The correspondence between CPU interface and the shared pin is as follows.

Pin Name	Parallel Interface (SER_N=H)	Serial Interface (SER_N=L)
D7-0	D7-0	Not used (Fixed to “H” or “L”)
PS2-0	PS2-0	Not used (Fixed to “H” or “L”)
CS_N	CS_N	SCS_N
RD_N	RD_N	SDIN
WR_N	WR_N	SCLK
WAIT_N	WAIT_N	SDOUT
READY_N	READY_N	Not used (N.C.)
INT_N	INT_N	INT_N

ii) Sharing of Digital Video Input Pins

YGV638 supports the digital video input of RGB666, 16bit YCrCb, and 8bit YCrCb format. The correspondence between the format of digital video and the pins are as follows.

Pin Name	RGB666 (DVIF=2’b00)	8bit YCrCb (DVIF=2’b01)	16bit YCrCb (DVIF=2’b10)
DRI2	DRI2	Not used	CIN0
DRI3	DRI3	Not used	CIN1
DRI4	DRI4	Not used	CIN2
DRI5	DRI5	Not used	CIN3
DRI6	DRI6	Not used	CIN4
DRI7	DRI7	Not used	CIN5
DGI2	DGI2	Not used	CIN6
DGI3	DGI3	Not used	CIN7
DGI4	DGI4	Not used	Not used
DGI5	DGI5	Not used	Not used
DGI6	DGI6	DIN0	YIN0
DGI7	DGI7	DIN1	YIN1
DBI2	DBI2	DIN2	YIN2
DBI3	DBI3	DIN3	YIN3
DBI4	DBI4	DIN4	YIN4
DBI5	DBI5	DIN5	YIN5
DBI6	DBI6	DIN6	YIN6
DBI7	DBI7	DIN7	YIN7
DGCKIN	DGCKIN	DGCKIN	DGCKIN
DVSIN_N	DVSIN_N	Not used	DVSIN_N
DHSIN_N	DHSIN_N	Not used	DHSIN_N

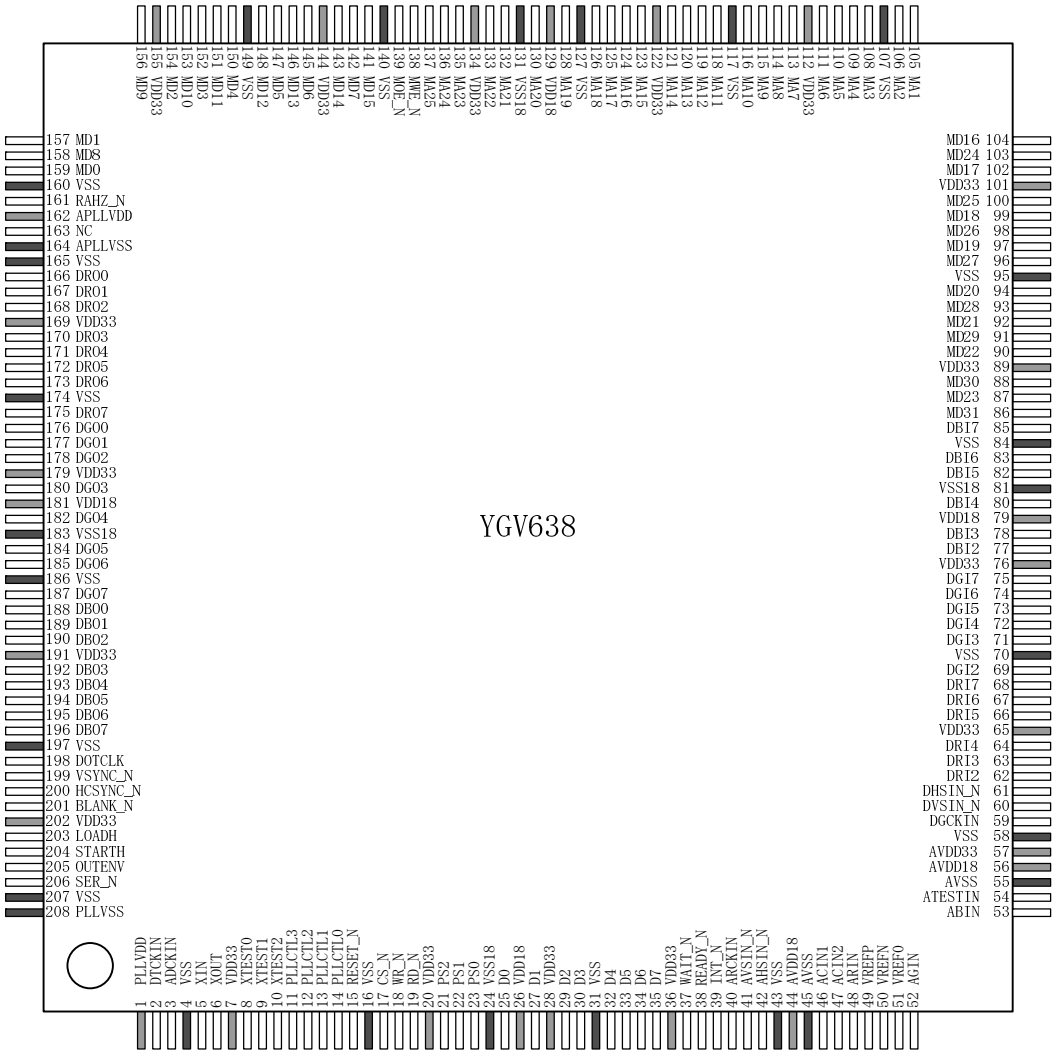
Pull up the “Not used” pins to “H” or “L” outside the device.

iii) Sharing of Monitor Interface Pins

YGV638 has an on-chip LCD timing controller. The function of the following pins depends on whether or not the timing controller is used, as shown below:

Pin Name	Timing controller not used (TCONE=0)	Timing controller used (TCONE=1)
DRO7-0	DRO7-0	DRO7-0
DGO7-0	DGO7-0	DGO7-0
DBO7-0	DBO7-0	DBO7-0
DOTCLK	DOTCLK	DOTCLK
HCSYNC_N	HCSYNC_N	CLKV
VSYNC_N	VSYNC_N	POL
BLANK_N	BLANK_N	STARTV
LOADH	Not used	LOADH
STARTH	Not used	STARTH
OUTENV	Not used	OUTENV

● Pin Assignments

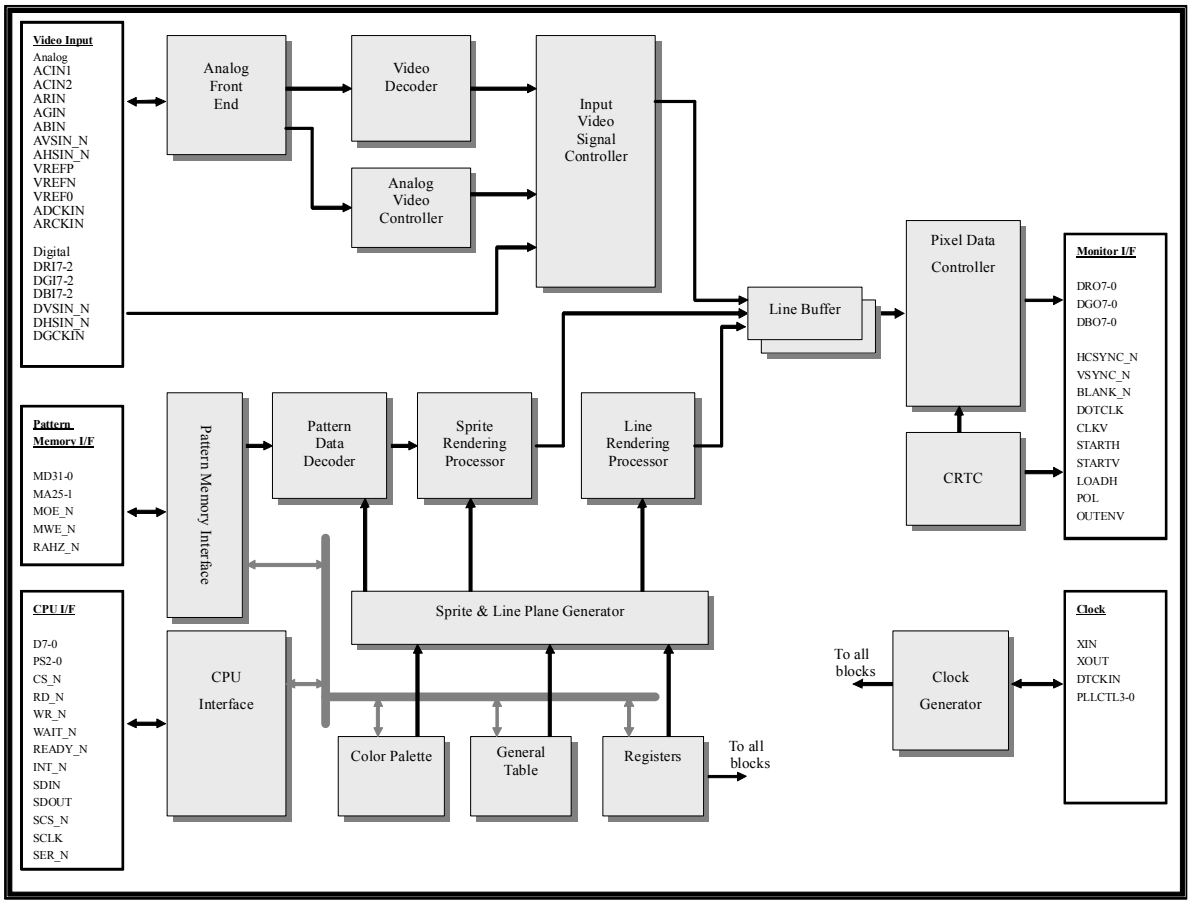


<208pin LQFP Top View>

■ Pin Names

#	Pin Name	#	Pin Name	#	Pin Name	#	Pin Name
1	PLLVDD	53	ABIN	105	MA1	157	MD1
2	DTCKIN	54	ATESTIN	106	MA2	158	MD8
3	ADCKIN	55	AVSS	107	VSS	159	MD0
4	VSS	56	AVDD18	108	MA3	160	VSS
5	XIN	57	AVDD33	109	MA4	161	RAHZ_N
6	XOUT	58	VSS	110	MA5	162	APLLVDD
7	VDD33	59	DGCKIN	111	MA6	163	NC
8	XTEST0	60	DVSIN_N	112	VDD33	164	APLLVSS
9	XTEST1	61	DHSIN_N	113	MA7	165	VSS
10	XTEST2	62	DRI2	114	MA8	166	DRO0
11	PLLCTL3	63	DRI3	115	MA9	167	DRO1
12	PLLCTL2	64	DRI4	116	MA10	168	DRO2
13	PLLCTL1	65	VDD33	117	VSS	169	VDD33
14	PLLCTL0	66	DRI5	118	MA11	170	DRO3
15	RESET_N	67	DRI6	119	MA12	171	DRO4
16	VSS	68	DRI7	120	MA13	172	DRO5
17	CS_N	69	DGI2	121	MA14	173	DRO6
18	WR_N	70	VSS	122	VDD33	174	VSS
19	RD_N	71	DGI3	123	MA15	175	DRO7
20	VDD33	72	DGI4	124	MA16	176	DGO0
21	PS2	73	DGI5	125	MA17	177	DGO1
22	PS1	74	DGI6	126	MA18	178	DGO2
23	PS0	75	DGI7	127	VSS	179	VDD33
24	VSS18	76	VDD33	128	MA19	180	DGO3
25	D0	77	DBI2	129	VDD18	181	VDD18
26	VDD18	78	DBI3	130	MA20	182	DGO4
27	D1	79	VDD18	131	VSS18	183	VSS18
28	VDD33	80	DBI4	132	MA21	184	DGO5
29	D2	81	VSS18	133	MA22	185	DGO6
30	D3	82	DBI5	134	VDD33	186	VSS
31	VSS	83	DBI6	135	MA23	187	DGO7
32	D4	84	VSS	136	MA24	188	DBO0
33	D5	85	DBI7	137	MA25	189	DBO1
34	D6	86	MD31	138	MWE_N	190	DBO2
35	D7	87	MD23	139	MOE_N	191	VDD33
36	VDD33	88	MD30	140	VSS	192	DBO3
37	WAIT_N	89	VDD33	141	MD15	193	DBO4
38	READY_N	90	MD22	142	MD7	194	DBO5
39	INT_N	91	MD29	143	MD14	195	DBO6
40	ARCKIN	92	MD21	144	VDD33	196	DBO7
41	AVSIN_N	93	MD28	145	MD6	197	VSS
42	AHSIN_N	94	MD20	146	MD13	198	DOTCLK
43	VSS	95	VSS	147	MD5	199	VSYNC_N
44	AVDD18	96	MD27	148	MD12	200	HCSYNC_N
45	AVSS	97	MD19	149	VSS	201	BLANK_N
46	ACIN1	98	MD26	150	MD4	202	VDD33
47	ACIN2	99	MD18	151	MD11	203	LOADH
48	ARIN	100	MD25	152	MD3	204	STARTH
49	VREFP	101	VDD33	153	MD10	205	OUTENV
50	VREFN	102	MD17	154	MD2	206	SER_N
51	VREF0	103	MD24	155	VDD33	207	VSS
52	AGIN	104	MD16	156	MD9	208	PLLVSS

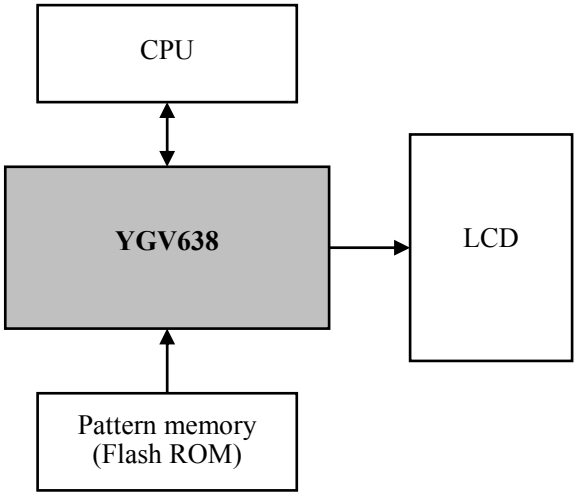
■ Block Diagram



● Typical Applications

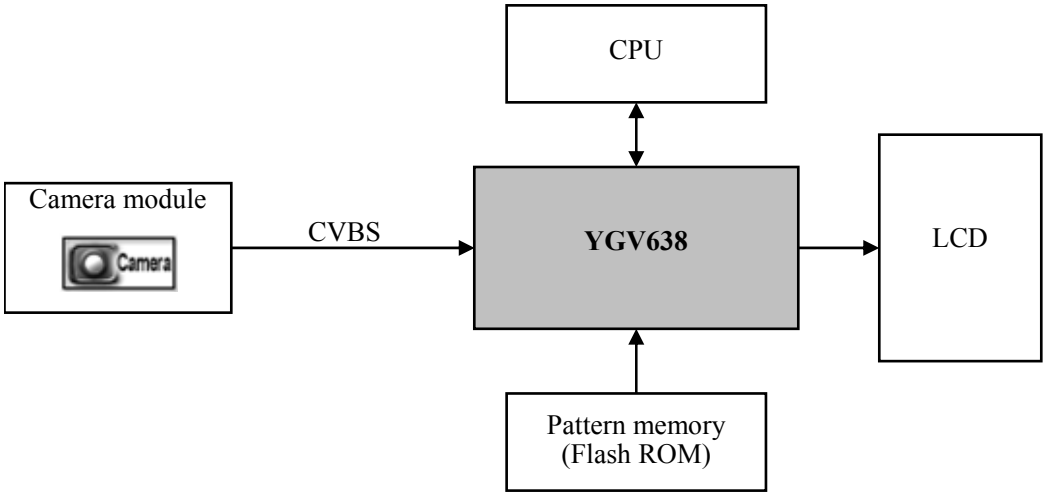
■ YGV638 Stand-alone system

Typical display contents: Dashboard instruments or vehicle information and alarms



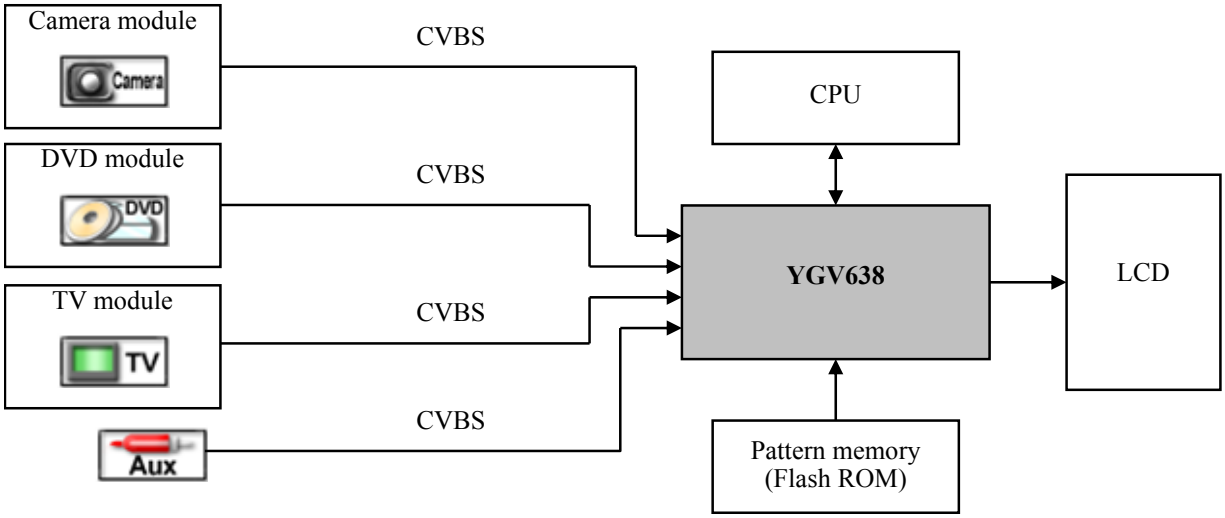
■ OSD system for video camera images

Typical display contents: Dashboard instruments or vehicle information and alarms, Blind spot monitor, Night view



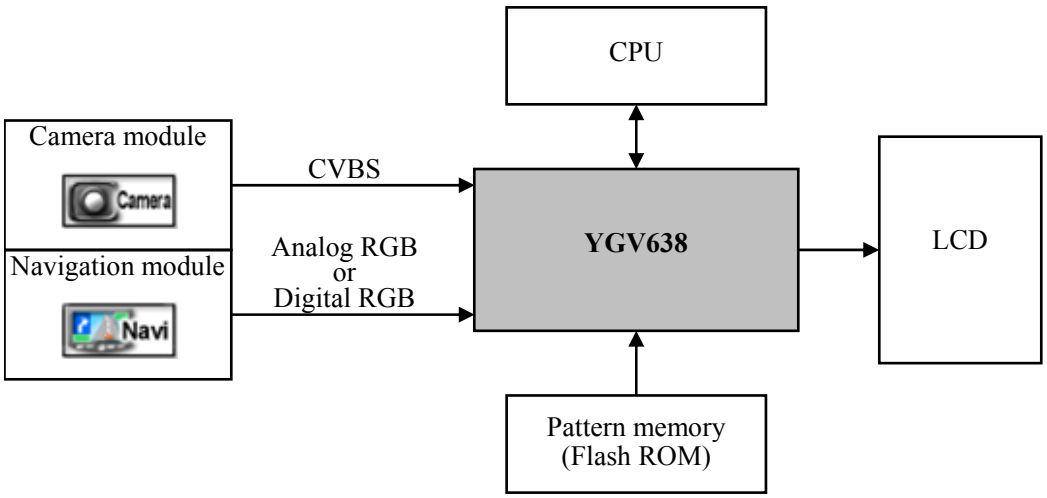
■ AV + Video camera images

Typical display contents: Dashboard instruments and vehicle information, Blind spot monitor, HMI (Air-conditioner, Audio), DVD, TV, AUX



■ Video camera add-ons for car navigation systems

Typical display contents: Dashboard instruments and vehicles information, Blind spot monitor, HMI (Air-conditioner, Audio), Car navigation system, Video



■ Electrical Characteristics

● Absolute Maximum Ratings

Items	Symbol	Ratings	Unit	Note
Power supply voltage (VDD33 pin)	V_{DD33}	-0.5 to +4.6	V	1
Power supply voltage (VDD18 pin)	V_{DD18}	-0.5 to +2.5	V	1
Analog power supply voltage (AVDD33 pin)	V_{AVD33}	-0.5 to +4.6	V	1
Analog power supply voltage (AVDD18 pin)	V_{AVD18}	-0.5 to +2.5	V	1
PLL power supply voltage (PLLVDD, APLLVDD pin)	V_{PLVD}	-0.5 to +2.5	V	1
Input pin voltage (Tolerant pin)	V_I	-0.5 to VDD33+4.6 (≤ 5.5 Max)	V	1
Input pin voltage (Analog pin)	V_I	-0.5 to AVDD+0.5 (≤ 4.6 Max)	V	1
Input pin voltage (Other pin)	V_I	-0.5 to VDD33+0.5 (≤ 4.6 Max)	V	1
Output pin voltage (Tolerant pins including I/O pins)	V_O	-0.5 to VDD33+4.6 (≤ 5.5 Max)	V	1
Output pin voltage (Analog pins including I/O pins)	V_O	-0.5 to AVDD+0.5 (≤ 4.6 Max)	V	1
Output pin voltage (Other pins including I/O pins)	V_O	-0.5 to VDD33+0.5 (≤ 4.6 Max)	V	1
Input pin current	I_I	-20 to +20	mA	
Output pin current	I_O	-20 to +20	mA	
Storage temperature	T_{STG}	-50 to +125	℃	

Note 1) Voltage relative to V_{SS}=0V.

● Recommended Operating Condition

Items	Symbol	Min.	Typ.	Max.	Unit	Note
Power supply voltage (VDD33 pin)	V_{DD33}	3.0	3.3	3.6	V	1
Power supply voltage (VDD18 pin)	V_{DD18}	1.65	1.8	1.95	V	1
Analog power supply voltage (AVDD33 pin)	V_{AVD33}	3.0	3.3	3.6	V	1
Analog power supply voltage (AVDD18 pin)	V_{AVD18}	1.65	1.8	1.95	V	1
PLL power supply voltage (PLLVDD, APLLVDD pin)	V_{PLVD} V_{APVD}	1.65	1.8	1.95	V	1
Operating ambient temperature	T_{OP}	-40		85	℃	2

Note 1) Voltage relative to V_{SS}=0V.

Note 2) The ambient temperature of 85℃ is the value measured under the following conditions:
Four-layer board with over 300% copper trace coverage

● Current Consumption

Items	Conditions	Symbol	Min.	Typ.	Max.	Unit	Note
Total power consumption	C_L=20pF V_{IL}=GND V_{IH}=V_{DD33}	P_D			766	mW	1
Current consumption by supply voltage							
VDD18 (including PLLVDD, APLLVDD)		I_{VD18}			192	mA	1, 2
VDD33		I_{VDD33}			40	mA	1
AVDD33		I_{AVD33}			20	mA	1
AVDD18		I_{AVD18}			90	mA	1

Note 1) Current consumption value and power consumption value are the values under the recommended operating condition.

Note 2) PLLVDD and APLLVDD are internally connected to VDD18.

● DC Characteristics

Items	Symbol	Min.	Typ.	Max.	Unit	Note
Low level input voltage (XIN pin)	V_{IL}	-0.3		$0.3\times V_{DD33}$	V	1
Low level input voltage (except XIN pin)	V_{IL}	-0.3		0.8	V	1
High level input voltage (XIN pin)	V_{IH}	$0.7\times V_{DD33}$		V_{DD33}+0.3	V	1
High level input voltage (RESET_N pin)	V_{IH}	2.2		5.5	V	1, 2
High level input voltage (Tolerant pin other than RESET_N)	V_{IH}	2.0		5.5	V	1, 2
High level input voltage (except the above)	V_{IH}	2.0		V_{DD33}+0.3	V	1

Note 1) Voltage relative to V_{SS}=0V.

Note 2) 5.5V can be applied to the Tolerant pin when the supply voltage is within the range of the recommended operating voltage; however, up to 3.6V when the power is not applied.

Items	Conditions	Symbol	Min.	Typ.	Max.	Unit	Note
Low level output voltage (except XOUT pin)	I_{OL}=100µA	V_{OL}	0		0.2	V	1
	I_{OL}=2mA	V_{OL}	0		0.4	V	1
High level output voltage (except XOUT pin)	I_{OH}= -100µA	V_{OH}	V_{DD33}-0.2		V_{DD33}	V	1
	I_{OH}= -2mA	V_{OH}	2.4		V_{DD33}	V	1
Input leak current		I_{LI}	-10		+10	µA	
Output leak current		I_{LO}	-25		+25	µA	

Note 1) Voltage relative to V_{SS}=0V.

Items	Symbol	Min.	Typ.	Max.	Unit	Note
Analog video input voltage (ACIN1, ACIN2 pins)	V_{ACIN}		1.25	1.4	Vp-p	1
Analog video input voltage (ARIN, AGIN, ABIN pins)	V_{ARIN}		0.7	1.4	Vp-p	1

Note 1) The above maximum value is for the setting of "R#021h: ADC*GAIN=2'b00."

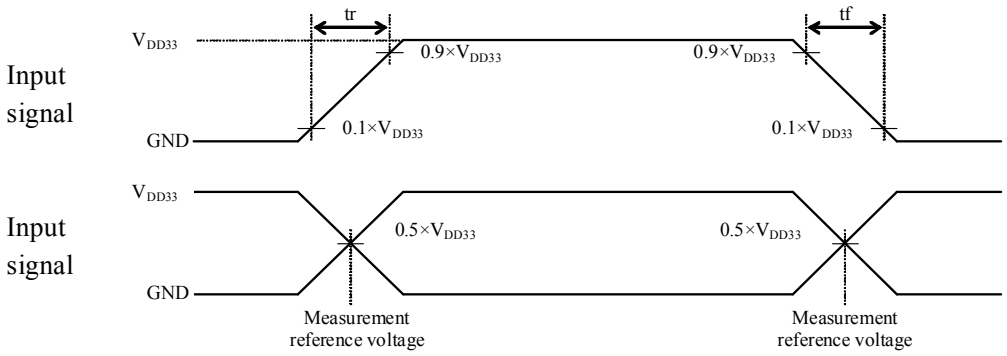
Items	Symbol	Min.	Typ.	Max.	Unit	Note
Input pin capacitance	C_I			10	pF	
Output pin capacitance	C_O			10	pF	
Input-Output pin capacitance	C_{IO}			10	pF	

● AC Characteristics

AC characteristic is a value under the following conditions unless otherwise noted.

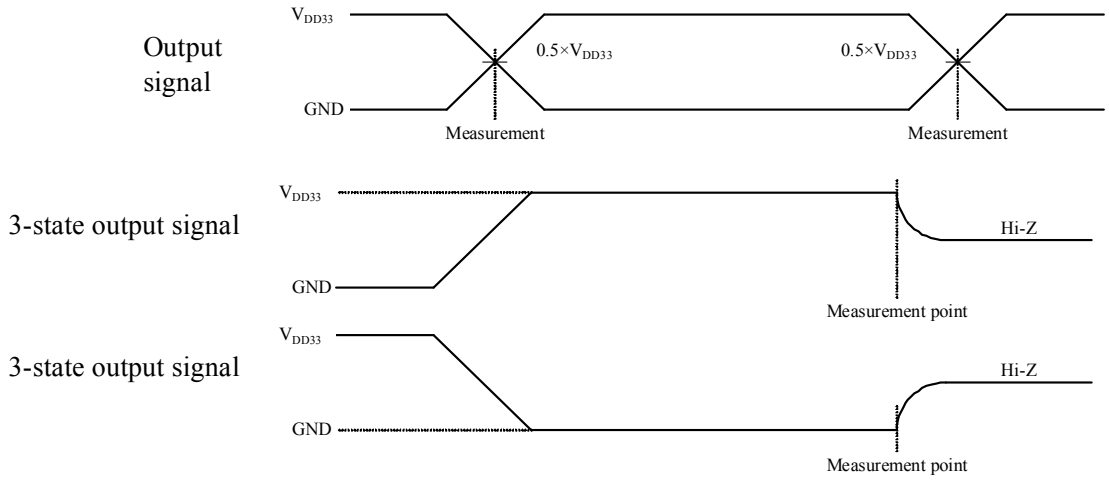
■ Input signal measurement condition:

Input voltages	0V / V_{DD33}
Input transition time (tr, tf)	1ns (Provide for the transition time between 10% and 90% of the input voltage.)
Input measurement reference voltage	0.5×V_{DD33}

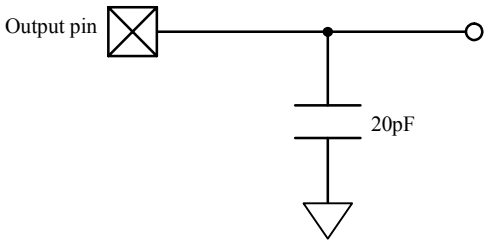


■ Output signal measurement condition

Output measurement reference voltage	0.5×V_{DD33} (In neither 3-state output pin nor input output pins, even when it changed to high impedance, an output wave changes; therefore, I/O cell specifies the transition to high impedance to the timing, being as a disable state.)



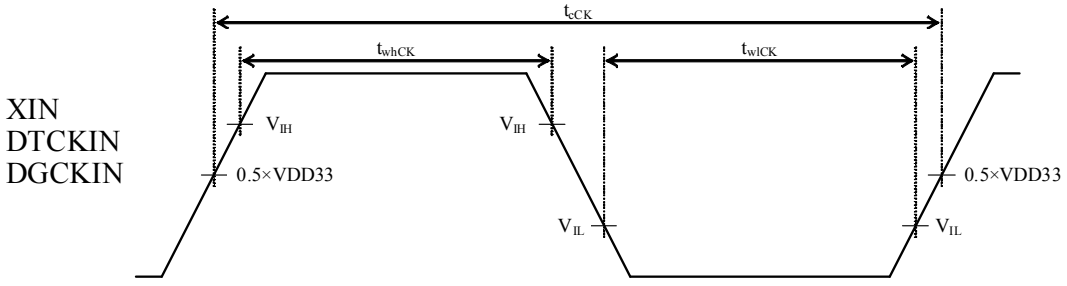
Output load capacitance 20pF

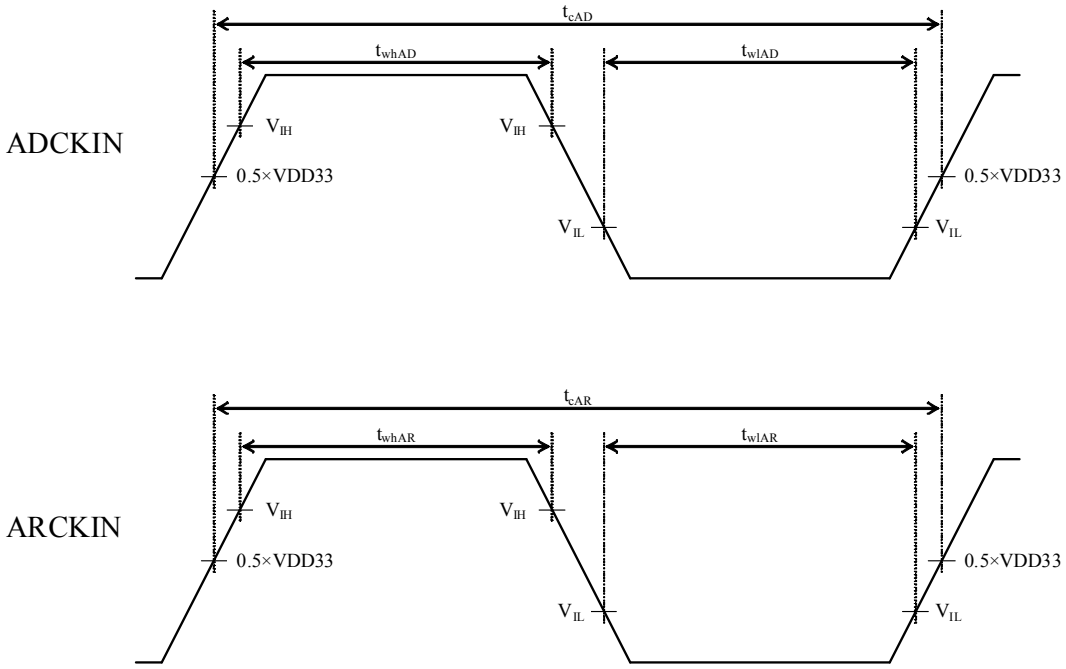


· Clock Input

No.	Items	Symbol	Min.	Typ.	Max.	Unit	Note
1	XIN, DTCKIN, DGCKIN: clock frequency	f_{CK}	6		40	MHz	1
	XIN, DTCKIN, DGCKIN: clock cycle time	t_{cCK}	25		166	ns	
2	XIN, DTCKIN, DGCKIN: clock high level pulse width	t_{whCK}	7.5			ns	
3	XIN, DTCKIN, DGCKIN: clock low level pulse width	t_{wlCK}	7.5			ns	
4	ADCKIN: clock frequency	f_{AD}	20		28	MHz	
	ADCKIN: clock cycle time	t_{cAD}	35.7		50	ns	
5	ADCKIN: clock high level pulse width	t_{whAD}	14.29			ns	
6	ADCKIN: clock low level pulse width	t_{wlAD}	14.29			ns	
7	ARCKIN: clock frequency	f_{AR}	6		40	MHz	
	ARCKIN: clock cycle time	t_{cAR}	25		166	ns	
8	ARCKIN: clock high level pulse width	t_{whAR}	10			ns	
9	ARCKIN: clock low level pulse width	t_{wlAR}	10			ns	
10	SYCLK: clock frequency	f_{SY}	63		84	MHz	2
	SYCLK: clock cycle time	t_{cSY}	11.90		15.88	ns	2
11	DCLK: clock frequency	f_{DT}	6		40	MHz	2
	DCLK: clock cycle time	t_{cDT}	25		166	ns	2

Note 1) The maximum of the oscillation frequency between XIN-XOUT is 30 MHz.
Note 2) SYCLK, DCLK is the internal clock.





· Power Supply and Reset Input

No.	Items	Symbol	Min.	Typ.	Max.	Unit	Note
1	RESET_N: input time	t_{wRES}	10			μs	1
2	CPU access stand-by time after RESET_N negation	t_{wAW}	1 to 6.7			ms	2
3	RESET_N: setup time	t_{sRES}	0			ns	3
4	Power-on time difference	t_{VSKWR}			1	s	4
5	Power-off time difference	t_{VSKWF}			1	s	5
6	Power rise time	t_{VRISE}			200	ms	

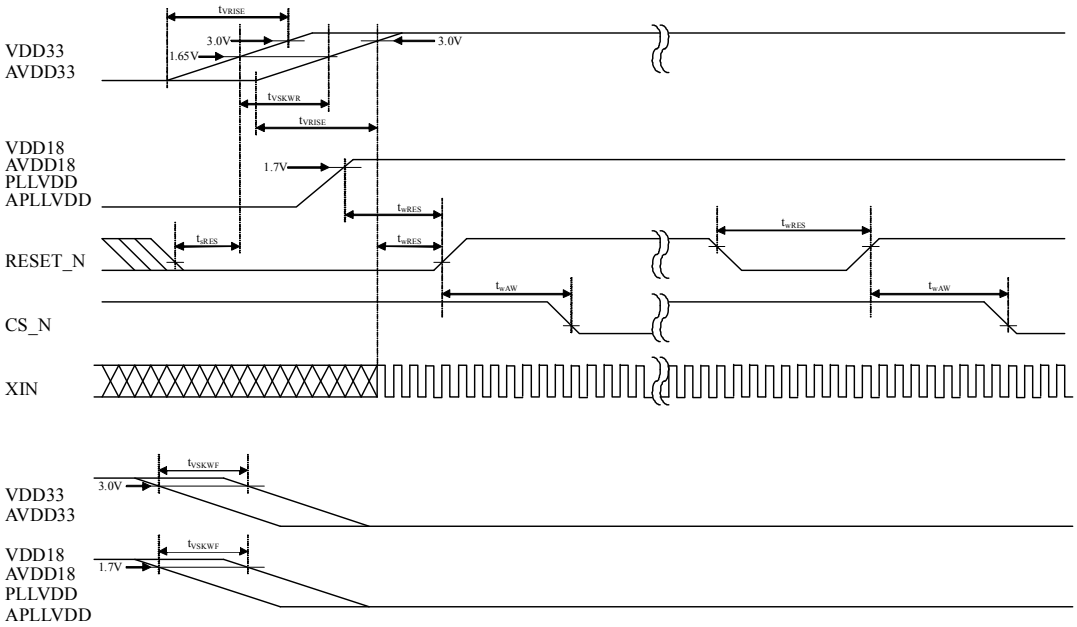
Note 1) The time from a point where a power supply powered up last VDD33 reaches at 3.0V, and VDD18 reaches at 1.7V, and the input clock to the XIN pin becomes stable.

Note 2) It is necessary to wait to access for 40000 × t_XIN time (cycle of the clock inputted into XIN pin) after RESET_N negation as PLL lock-up time.

Note 3) The specified value of VDD which is raised up the earliest.

Note 4) It is preferable to turn on VDD33, VDD18, AVDD33, AVDD18, PLLVDD, and APLLVDD at the same time. If 1 second or more time-difference occurs among their power-on, it may affect the LSI's reliability.

Note 5) It is preferable to turn off VDD33, VDD18, AVDD33, AVDD18, PLLVDD, and APLLVDD at the same time. If 1 second or more time-difference occurs among their power-off, it may affect the LSI's reliability.



· CPU Interface

i) Parallel Interface

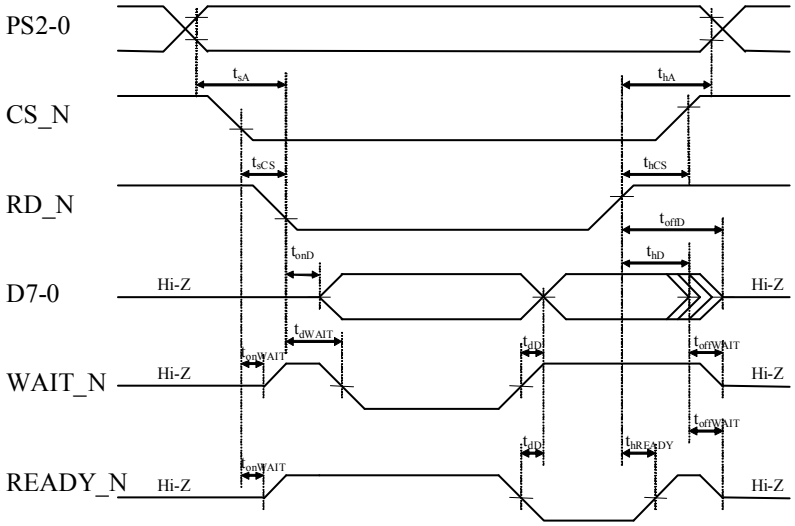
No.	Items	Symbol	Min.	Typ.	Max.	Unit	Note
1	PS2-0: setup time	tsA	4			ns	1
2	PS2-0: hold time	thA	0				1
3	CS_N: setup time	tsCS	0				2
4	CS_N: hold time	t_{hCS}	0				2
5	D7-0: output data turn on time	t_{onD}	0				
6	D7-0: output data turn off time	t_{offD}			30		
7	D7-0: output data valid delay time	t_{dD}			0		
8	D7-0: output data hold time	t_{hD}	0				
9	WAIT_N, READY_N: turn on time	t_{onWAIT}	0				
10	WAIT_N: valid delay time	t_{dWAIT}			25		
11	WAIT_N, READY_N: turn off time	$t_{offWAIT}$			30		
12	D7-0: input data setup time	t_{sD}	t_{cSY}+15				
13	D7-0: input data hold time	t_{hD}	0				
14	WR_N: hold time	t_{hWR}	0				
15	READY_N: hold time	t_{hREADY}	0		30		
16	command pulse active time	t_{aCMD}	$2 \times t_{cSY}$				3
17	command pulse inhibit time	t_{iCMD}	$4 \times t_{cSY}$				3
18	command cycle time	t_{cCMD}	$6 \times t_{cSY}$				3

Note 1) Specified values for WR_N and RD_N signals; however, in CS_N control, there are specified values for CS_N.

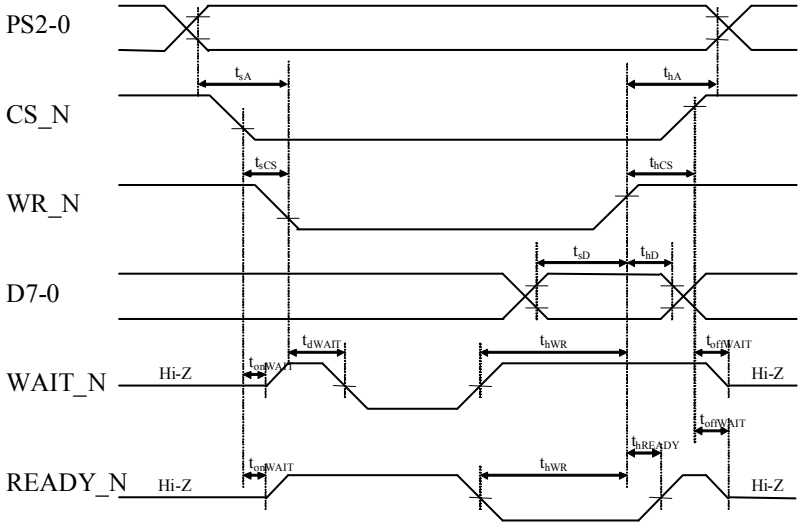
Note 2) Conditions that prove to be WR_N and RD_N controls. If these specified values are not met, these are for CS_N control.

Note 3) “command pulse” means a low active pulse obtained by performing OR operation between CS_N signal and each of WR_N and RD_N signals.

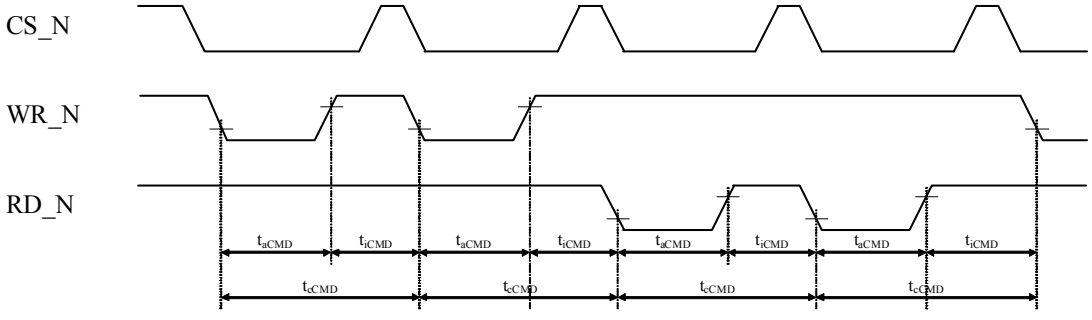
- CPU read cycle



- CPU write cycle



- Access cycle



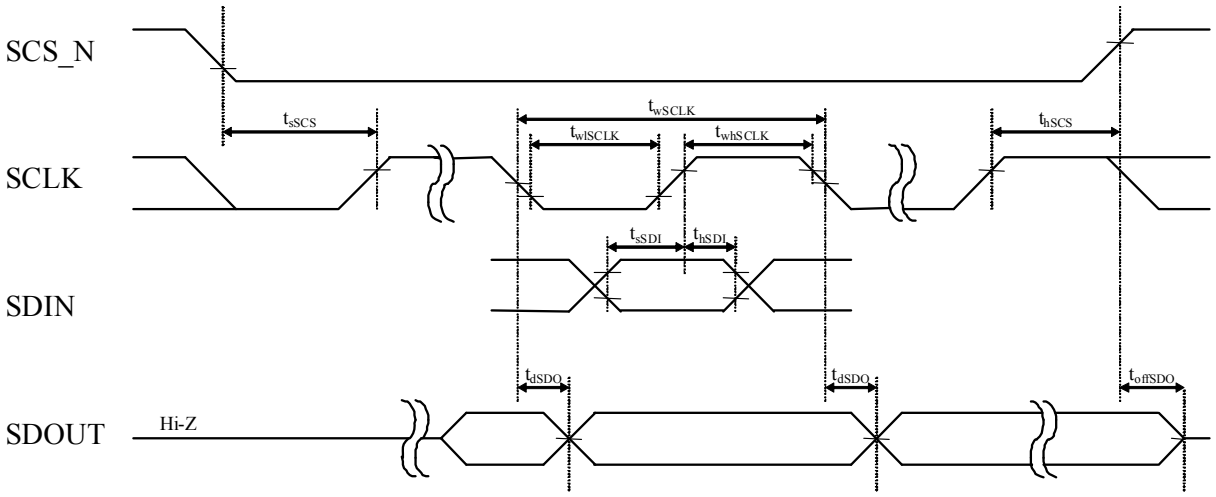
ii) Serial Interface

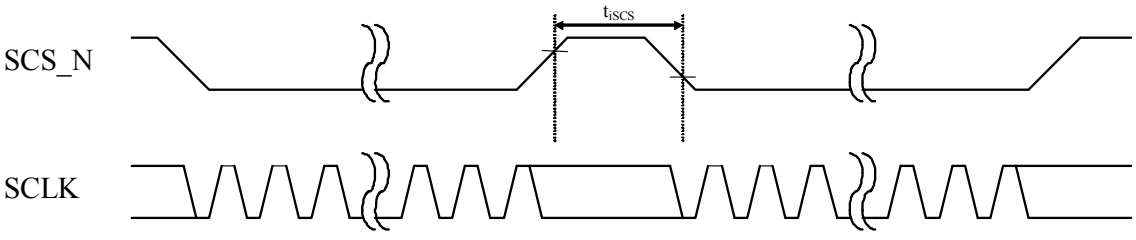
No.	Items	Symbol	Min.	Typ.	Max.	Unit	Note
1	SCLK clock cycle time	t_{wSCLK}	200			ns	
			$4 \times t_{cXIN}$				1, 2
2	SCLK clock high level pulse width	t_{whSCLK}	100				
			$2 \times t_{cXIN}$				1, 2
3	SCLK clock low level pulse width	t_{wlSCLK}	100				
			$2 \times t_{cXIN}$				1, 2
4	SCS_N: setup time	t_{sSCS}	25				
5	SCS_N: hold time	t_{hSCS}	25				
6	SDIN: setup time	t_{sSDI}	25				
7	SDIN: hold time	t_{hSDI}	25				
8	SDOUT: output data delay time	t_{dSDO}			65		3
9	SDOUT: turn off time	t_{offSDO}			20		
10	SCS_N: pulse inhibit time	t_{iSCS}			400		

Note 1) Alternative value during YGV638 initialization.

Note 2) tc_{XIN} is the period of a clock that is fed to XIN pin.

Note 3) During YGV638 initialization, the maximum of t_{dSDO} becomes 17 ns plus 3 times the XIN input cycle.



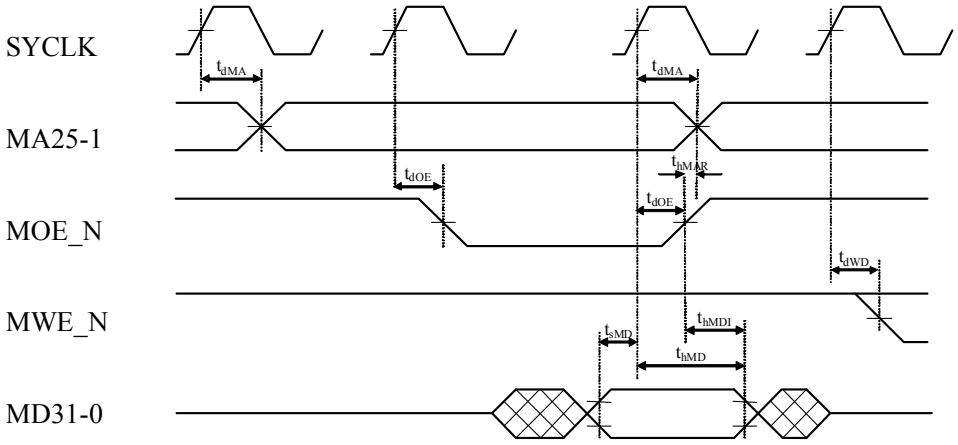


· Pattern Memory Interface

No.	Items	Symbol	Min.	Typ.	Max.	Unit	Note
1	MA25-1: output delay time	t_{dMA}			14	ns	1
2	MOE_N: output delay time	t_{dOE}	2		14		1
3	MWE_N: output delay time	t_{dWE}	2		14		1
4	MD31-0: input setup time	t_{sMD}	4				1
5	MD31-0: input hold time	t_{hMD}	0				1
6	MD31-0: output delay time	t_{dMD}			24		1
7	MA25-1: output hold time from MOE_N	t_{hMAR}	0				
8	MD31-0: input hold time from MOE_N and MA25-1	t_{hMDI}	0				
9	MA25-1: output hold time from MWE_N	t_{hMAW}	0				
10	MD31-0: output hold time from MWE_N	t_{hMDO}	1				
11	MD31-0: turn off time from MWE_N	t_{offMDO}	1		10		
12	output turn off / on time from RAHZ_N	$t_{on/offRA}$			25		

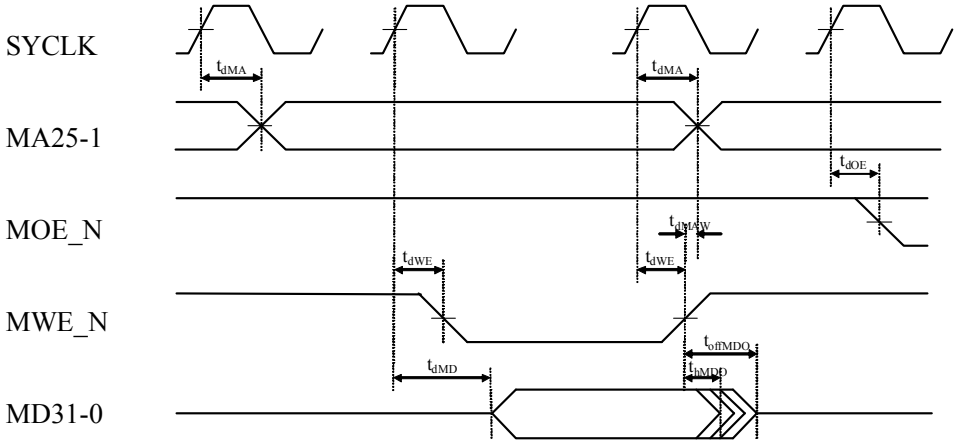
Note 1) Specified value for an internal clock (SYCLK)

- Memory Access Cycle (Random Read Cycle)



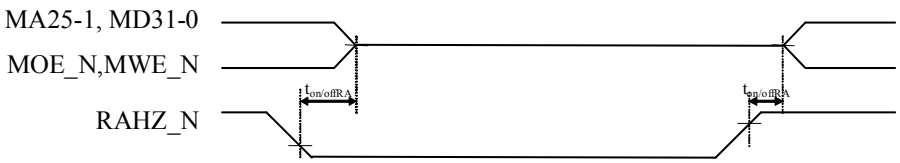
Note) After the read access, values of MA[25:0] and MOE_N are held until the next access to the pattern memory.

- Memory Access Cycle (Write Cycle)



Note) After the write access, values of MA25–1 and MOE_N are held until the next access to the pattern memory.

- RAHZ_N



- AC Characteristics of the External Memory Connected to YGV638

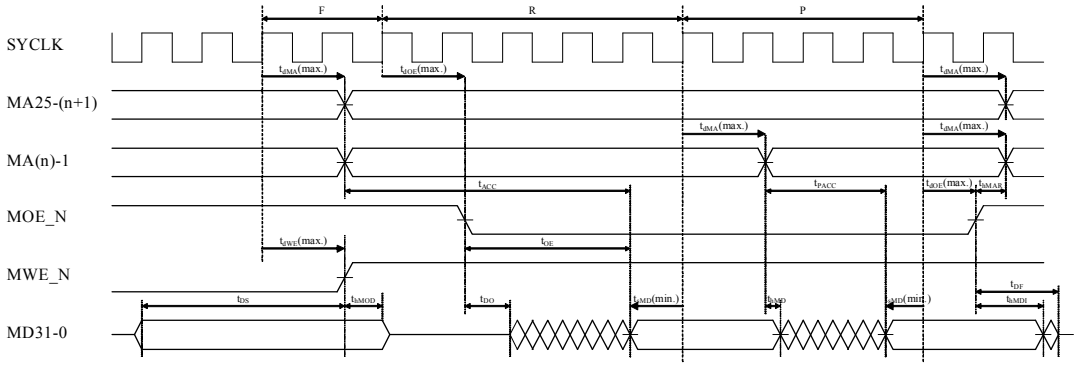
AC characteristics of the external memory connected to YGV638 must meet the following conditions. (The following conditions are the values converted from the AC characteristics of the YGV638 Pattern Memory; they do not guarantee the following specifications directly. In addition, the item names below are those mainly for an externally-connected memory.)

"F", "R", and "P" in the below are as follows.

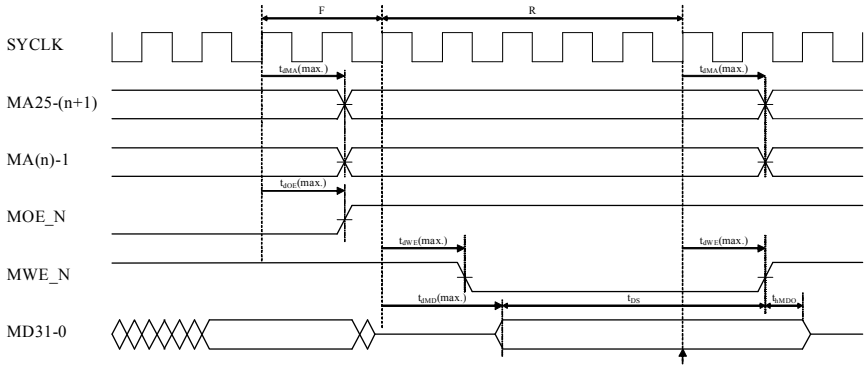
F = (R#008h: FLTIM[1:0] + 1) Number of floating clocks
R = (R#009h: RDM[3:0] + 1) Number of random access clocks
P = (R#009h: PAG[2:0] + 1) Number of page mode access clocks

No.	Items	Symbol	Conditions
13	Address access time	t_{ACC}	It should be (F + R) * t_{cSY} – t_{dMA}(max.) – t_{sMD}(min.) or less
14	Output enable time	t_{OE}	It should be R * t_{cSY} – t_{dOE}(max.) – t_{sMD}(min.) or less
15	Page mode access time	t_{PACC}	It should be P * t_{cSY} – t_{dMA}(max.) – t_{sMD}(min.) or less
16	Data turn on time	t_{DO}	It should be 0[ns] or over
17	Data turn off time	t_{DF}	It should be F * t_{cSY} - t_{dOE}(max.) + t_{dWE}(min.) or less
18	Data setup time	t_{DS}	It should be R * t_{cSY} - t_{dMD}(max.) + t_{dWE}(min.) or less

・Read Access Timing



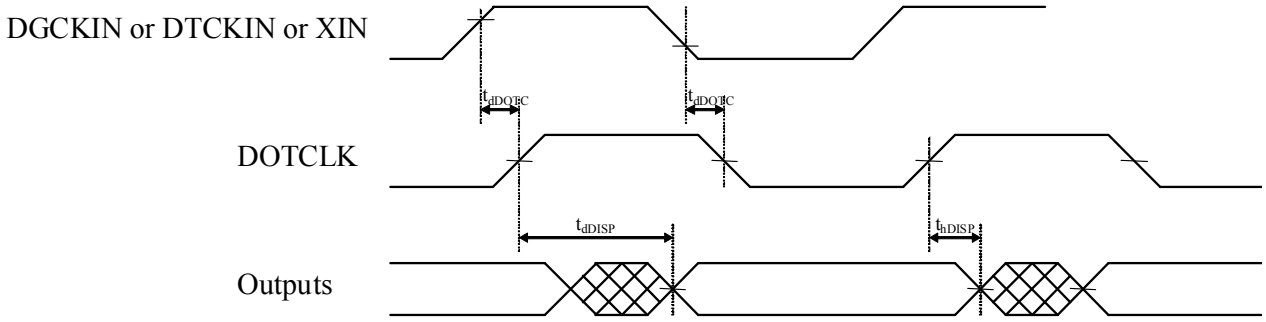
・Write Access Timing



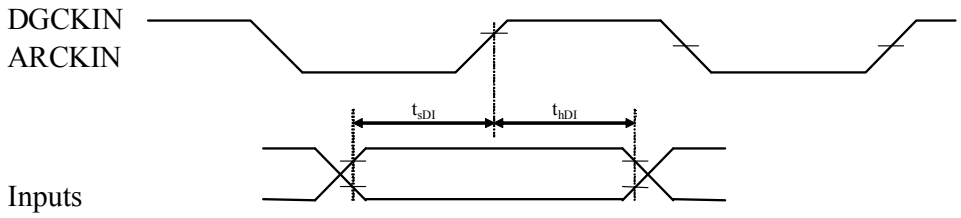
Note) After accesses, values of MA25–1 and MOE_N are held until the next access to the pattern memory.
Note) The value of R#008h: PGN[2:0] determines the "n" that apears in "MA25-(n+1)" and "MA(n)-1" in the figures.

· Video Signal Interface

No.	Items	Symbol	Min.	Typ.	Max.	Unit	Note
1	DOTCLK: delay time	t_{dDOTC}			26	ns	
2	VSYNC_N, HCSYNC_N, BLANK_N, DRO7-0, DGO7-0, DBO7-0, LOADH, STARTH, OUTENV: hold time	t_{hDISP}	0				
3	VSYNC_N, HCSYNC_N, BLANK_N, DRO7-0, DGO7-0, DBO7-0, LOADH, STARTH, OUTENV: delay time	t_{dDISP}			10		
4	DVSIN_N, DHSIN_N, DRI7-2, DGI7-2, DBI7-2: setup time	t_{sDI}	4				
5	DVSIN_N, DHSIN_N, DRI7-2, DGI7-2, DBI7-2: hold time	t_{hDI}	1				
6	AVSIN_N, AHSIN_N: setup time	t_{sDI}	3				
7	AVSIN_N, AHSIN_N: hold time	t_{hDI}	1				

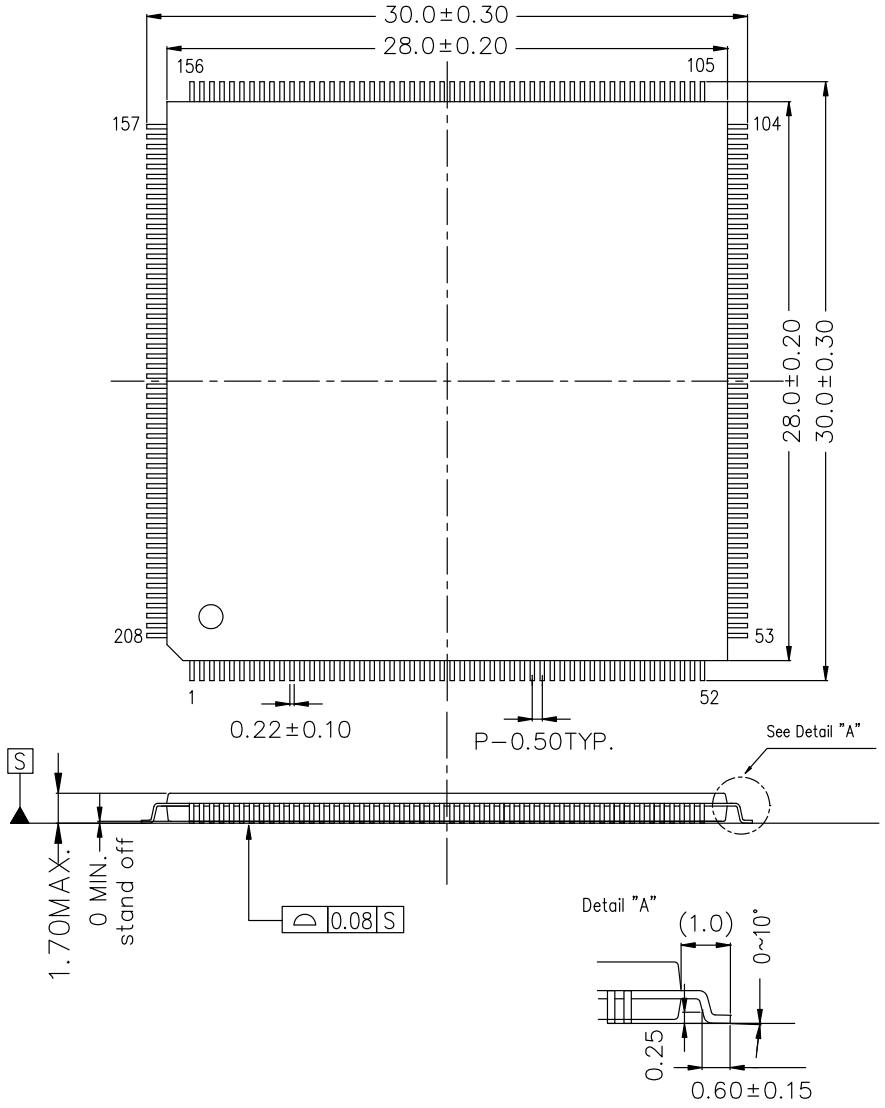


Note) the above figure shows the state that DOTCLK is not reversed.



■ Package Information

U-PK208VP1-16-1



端子厚さ/Lead Thickness 0.145±0.055

カッコ内の寸法値は参考値とする。
The value parenthesized is not specified.

モールド外形寸法はバリを含まない。
Plastic body dimensions do not include burr of resin.

UNIT: mm

注） 1. 表面実装LSIは、保管条件、および、半田付けについての特別な配慮が必要です。
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Note: 1. Special attention needs to be paid to the storage conditions and soldering method of the surface mount IC.
2. Dimension, form, etc. may differ depending on assembly plants.
For details, please contact your local Yamaha agent.

PRECAUTIONS AND INSTRUCTIONS FOR SAFETY

	WARNING
Prohibited	Do not use the device under stresses beyond those listed in Absolute Maximum Ratings. Such stresses may become causes of breakdown, damages, or deterioration, causing explosion or ignition, and this may lead to fire or personal injury.
Prohibited	Do not mount the device reversely or improperly and also do not connect a supply voltage in wrong polarity. Otherwise, this may cause current and/or power-consumption to exceed the absolute maximum ratings, causing personal injury due to explosion or ignition as well as causing breakdown, damages, or deterioration. And, do not use the device again that has been improperly mounted and powered once.
Prohibited	Do not short between pins. In particular, when different power supply pins, such as between high-voltage and low-voltage pins, are shorted, smoke, fire, or explosion may take place.
Instructions	As to devices capable of generating sound from its speaker outputs, please design with safety of your products and system in mind, such as the consequences of unusual speaker output due to a malfunction or failure. A speaker dissipates heat in a voice-coil by air flow accompanying vibration of a diaphragm. When a DC signal (several Hz or less) is input due to device failure, heat dissipation characteristics degrade rapidly, thereby leading to voice-coil burnout, smoking or ignition of the speaker even if it is used within the rated input value.

	CAUTION
Prohibited	Do not use Yamaha products in close proximity to burning materials, combustible substances, or inflammable materials, in order to prevent the spread of the fire caused by Yamaha products, and to prevent the smoke or fire of Yamaha products due to peripheral components.
Instructions	Generally, semiconductor products may malfunction and break down due to aging, degradation, etc. It is the responsibility of the designer to take actions such as safety design of products and the entire system and also fail-safe design according to applications, so as not to cause property damage and/or bodily injury due to malfunction and/or failure of semiconductor products.
Instructions	The built-in DSP may output the maximum amplitude waveform suddenly due to malfunction from disturbances etc. and this may cause damage to headphones, external amplifiers, and human body (the ear). Please pay attention to safety measures for device malfunction and failure both in product and system design.
Instructions	As semiconductor devices are not nonflammable, overcurrent or failure may cause smoke or fire. Therefore, products should be designed with safety in mind such as using overcurrent protection circuits to control the amount of current during operation and to shut off on failure.
Instructions	Products should be designed with fail safe in mind in case of malfunction of the built-in protection circuits. Note that the built-in protection circuits such as overcurrent protection circuit and high-temperature protection circuit do not always protect the internal circuits. In some cases, depending on usage or situations, such protection circuit may not work properly or the device itself may break down before the protection circuit kicks in.
Instructions	Use a robust power supply. The use of an unrobust power supply may lead to malfunctions of the protection circuit, causing device breakdown, personal injury due to explosion, or smoke or fire.
Instructions	Product's housing should be designed with the considerations of short-circuiting between pins of the mounted device due to foreign conductive substances (such as metal pins etc.). Moreover, the housing should be designed with spatter prevention etc. due to explosion or burning. Otherwise, the spattered substance may cause bodily injury.
Instructions	The device may be heated to a high temperature due to internal heat generation during operation. Therefore, please take care not to touch an operating device directly.

v02

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AGENT

YAMAHA CORPORATION

Address Inquiries to :
Semiconductor Sales & Marketing Department

■Head Office 203, Matsunokijima, Iwata,
Shizuoka, 438-0192, Japan
Tel. +81-539-62-4918 Fax.+81-539-62-5054

■Tokyo Office 2-17-11, Takanawa, Minato-ku,
Tokyo, 108-8586, Japan
Tel. +81-3-5488-5431 Fax.+81-3-5488-5088

■Osaka Office Universal City Wako Bldg.
6-2-82, Shimaya, Konohana-ku,
Osaka, 554-0024, Japan
Tel. +81-6-6465-0325 Fax.+81-6-6465-0391

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