Application manual how to connect ORTUS TECHNOLOGY LCD panels to Yamaha

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1. Outline

This document is intended to explain how to connect ORTUS TECHNOLOGY LCD panels to Yamaha GDCs (Graphic Display Controller) by describing the interface pins and the register settings of GDC (VC1D: YGV632). For more detailed information, please refer to its application manual.

※ For more information of VC1D or other Yamaha GDCs , please access the following URL.

http://www.yamaha.co.jp/english/product/lsi/graphic_controller/

2. List of ORTUS TECHNOLOGY LCD panels supported by VC1D

The followings are the list of the ORTUS TECHNOLOGY LCD panels supported by VC1D.

- COM37H3M04（3.7inch, 1,440[H]×640[V] dot, VGA/QVGA）
- COM65T6111 （6.5inch, 1,920[H]×480[V] dot, VGA）
- COM41T4148 （4.1inch, 960[H]×240[V] dot, QVGA）
- COM57T5135 （5.7inch, 960[H]×240[V] dot, QVGA）
- COM35H3827 （3.5inch, 720[H]×320[V] dot, QVGA, Portrait Type）

The LCD panels above are representatives of each group that has the same interface and the table below describes other LCD panels to have the same interface so that these can be also connected to VC1D.

A representative of ORTUS TECHNOLOGY LCD Panel	Other LCD panels with the same Interface
COM37H3M04	COM37H3M05, COM37H3M06, COM37H3M14
COM65T6111	COM65H6114, COM57T5132, COM57H5137, COM57T5M08, COM57H5M10
COM41T4148	COM22T2M59, COM22T2M74, COM35T3829, COM35T3831, COM35T3835, COM41T4150, COM41H4156, COM41T4M17, COM50T5123, COM50T5124, COM50H5125
COM57T5135	COM57H5139, COM57T5M04, COM57H5M06
COM35H3827	COM27H2M90, COM27H2N25, COM35H3833, COM35H3M09, COM35H3M10

3. ORTUS TECHNOLOGY LCD panels supported by VC1D

3.1. COM37H3M04

This chapter explains how to connect VC1D and COM37H3M04.

3.1.1. Pins Correspondence Table

LCD Panel Connector Pin No.	LCD Panel Pin Name	LCD Panel Pin Description	VC1D Pin No.	VC1D Pin Name
1	VSS	GND	-	-
2	VSS	GND	-	-
3	VDD	Power Supply	-	-
4	VDD	Power Supply	-	-
5	MODE	Mode Change Pin (Low: QVGA mode, High: VGA mode) [Notice：Do not change during operation.]	-	-
6	RESETB	Reset Signal (Low Active)	-	-
7	HSYNC	Horizontal Synch. (Negative Polarity)	135	HCSYNC_N
8	VSYNC	Vertical Synch. (Negative Polarity)	133	VSYNC_N
9	CLK	Dot Clock (Data sampling at falling edge)	137	DOTCLK
10	VSS	GND	-	-
11	D00	Display Data Input (B) 00h for Black Display D00: LSB D05:MSB Driver IC carries out gamma conversion internally.	125	DB0
12	D01		127	DB1
13	D02		128	DB2
14	D03		130	DB3
15	D04		131	DB4
16	D05		132	DB5
17	D10	Display Data Input (G) 00h for Black Display D00: LSB D05:MSB Driver IC carries out gamma conversion internally.	117	DG0
18	D11		119	DG1
19	D12		120	DG2
20	D13		121	DG3
21	D14		122	DG4
22	D15		124	DG5
23	D20	Display Data Input (R) 00h for Black Display D00: LSB D05:MSB Driver IC carries out gamma conversion internally.	110	DR0
24	D21		111	DR1
25	D22		112	DR2
26	D23		114	DR3
27	D24		115	DR4
28	D25		116	DR5
29	VSS	GND	-	-
30	DE	Input Data Effective Signal (Positive Polarity)	136	BLANK_N
31	STBYB	Stand-by Control Signal (Low: Stand-by Operation , High: Normal Operation)	-	-
32	TEST	Connect to VSS	-	-

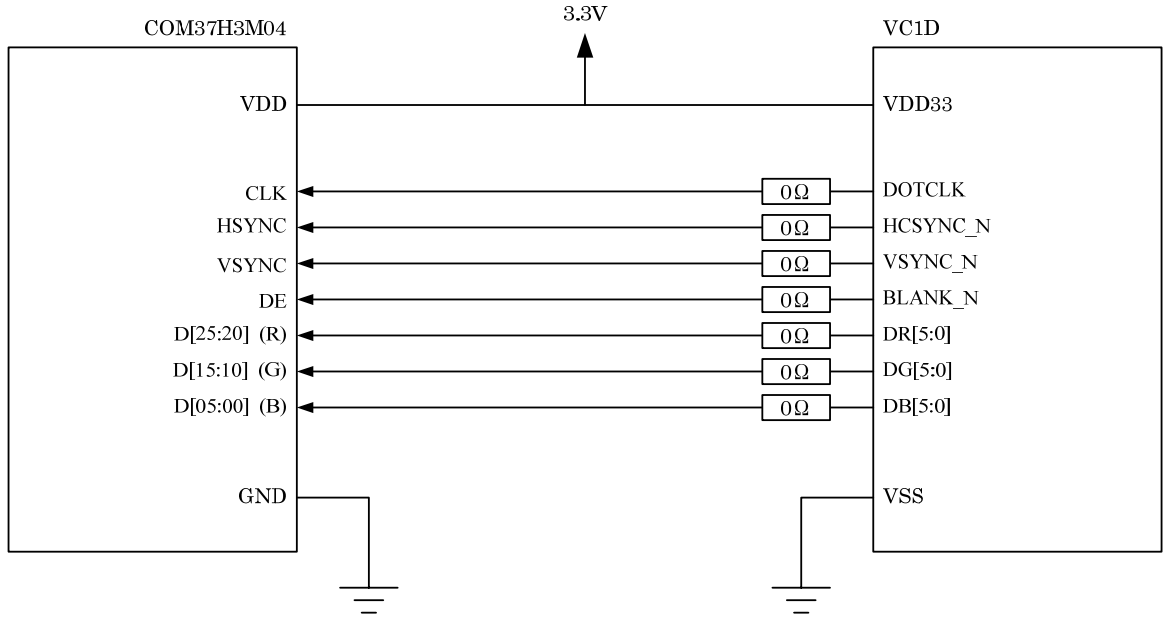
33	NC	OPEN	-	-
34	NC	OPEN	-	-
35	NC	OPEN	-	-
36	NC	OPEN	-	-
37	REV	Right/Left & Up/Down Display Reverse (Low: Normal Display, High: Reverse Display) [Notice: Do not change during operation]	-	-
38	BLH	Backlight Drive Source (Anode Side)	-	-
39	BLL	Backlight Drive Source (Cathode Side)	-	-

Notice) The following are the pins for VSS of VC1D.

Pin No.: 8, 19, 28, 32, 43, 51, 62, 72, 82, 93, 103, 113, 123, 134

※ The VDD range of COM37H3M04 needs to be +3.0V～+3.3V to adjust to the VDD33 range of VC1D which is +3.3V±0.3V.

3.1.2. Connection Diagram



※ The value of the dumping resistors needs to be adjusted to actual layout pattern.

3.1.3. Example of Register Settings

Both of VGA and QVGA are supported by COM37H3M04 and the following is an example of the register settings for VGA and QVGA and these settings needs to be modified according to customers' design.

- VGA（480×640） mode

R#04h: INTL	0	(0h)
R#04h: CSYPAL	0	(0h)
R#04h: CSYOE	0	(0h)
R#04h: REVSY	0	(0h)
R#04h－R#05h: VTL[9:0]	646	(286h)
R#06h－R#07h: HTL[10:0]	573	(23Dh)
R#08h－R#09h: VBLS[9:0]	643	(283h)
R#0Ah－R#0Bh: HBLS[10:0]	489	(1E9h)
R#0Ch－R#0Dh: VBLE[9:0]	3	(003h)
R#0Eh－R#0Fh: HBLE[10:0]	9	(009h)
R#10h－R#11h: VDS[9:0]	3	(003h)
R#12h－R#13h: HDS[10:0]	9	(009h)
R#14h－R#15h: VDE[9:0]	643	(283h)
R#16h－R#17h: HDE[10:0]	489	(1E9h)
R#18h: VSW[3:0]	0	(0h)
R#19: HSW[7:0]	1	(01h)

※ This is an example of the register settings when DOTCLK is 22.400MHz.

- QVGA（240×320）mode

R#04h: INTL	0	(0h)
R#04h: CSYPAL	0	(0h)
R#04h: CSYOE	0	(0h)
R#04h: REVSY	0	(0h)
R#04h－R#05h: VTL[9:0]	321	(141h)
R#06h－R#07h: HTL[10:0]	286	(11Eh)
R#08h－R#09h: VBLS[9:0]	323	(143h)
R#0Ah－R#0Bh: HBLS[10:0]	249	(0F9h)
R#0Ch－R#0Dh: VBLE[9:0]	3	(003h)
R#0Eh－R#0Fh: HBLE[10:0]	9	(009h)
R#10h－R#11h: VDS[9:0]	3	(003h)
R#12h－R#13h: HDS[10:0]	9	(009h)
R#14h－R#15h: VDE[9:0]	323	(143h)
R#16h－R#17h: HDE[10:0]	249	(0F9h)
R#18h: VSW[3:0]	0	(0h)
R#19: HSW[7:0]	1	(01h)

※This is an example of the register settings when DOTCLK is 5.600MHz.

3.2. COM65T6111

This chapter explains how to connect VC1D to COM37H3M04.

3.2.1. Pin Correspondence Table

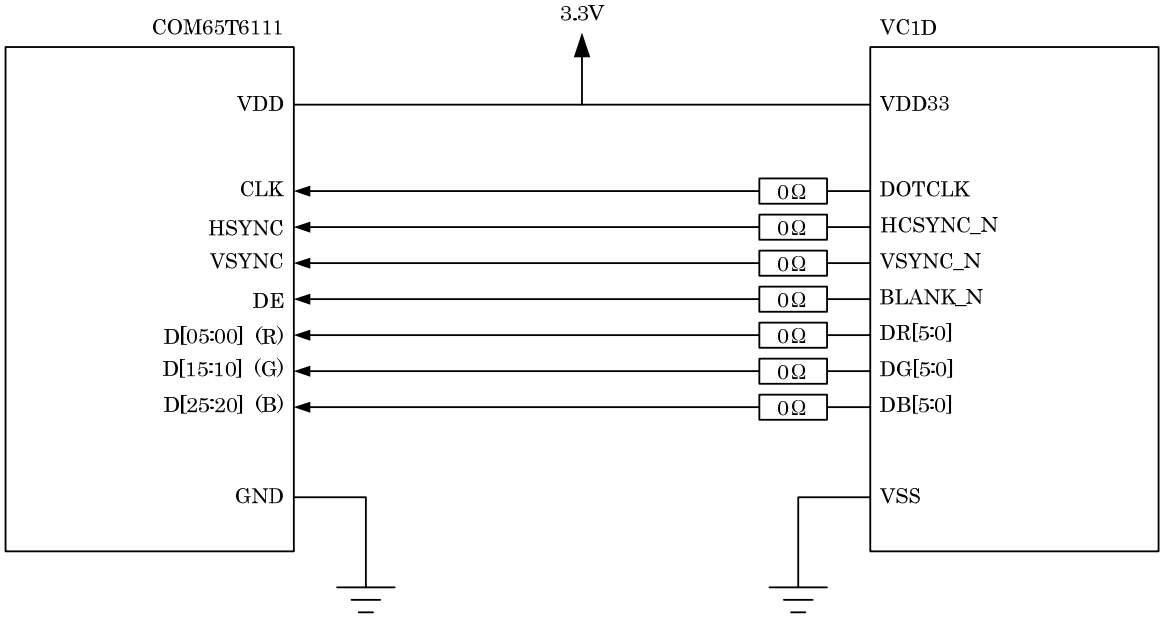
LCD Panel Connector Pin No.	LCD Panel Pin Name	LCD Panel Pin Description	VC1D Pin No.	VC1D Pin Name
1	VSS	GND	-	-
2	CLK	Dot Clock (Data sampling at rising edge)	137	DOTCLK
3	VSS	GND	-	-
4	HSYNC	Horizontal Synch. (Negative Polarity)	135	HCSYNC_N
5	VSYNC	Vertical Synch. (Negative Polarity)	133	VSYNC_N
6	VSS	GND	-	-
7	TEST1	Connect to VSS	-	-
8	TEST2	Connect to VSS	-	-
9	D20	Display Data Input (B) 00h for Black Display D20: LSB D25: MSB Driver IC carries out gamma conversion internally.	125	DB0
10	D21		127	DB1
11	D22		128	DB2
12	D23		130	DB3
13	D24		131	DB4
14	D25		132	DB5
15	VSS	GND	-	-
16	TEST3	Connect to VSS	-	-
17	TEST4	Connect to VSS	-	-
18	D10	Display Data Input (G) 00h for Black Display D20: LSB D25: MSB Driver IC carries out gamma conversion internally.	117	DG0
19	D11		119	DG1
20	D12		120	DG2
21	D13		121	DG3
22	D14		122	DG4
23	D15		124	DG5
24	VSS	GND	-	-
25	TEST5	Connect to VSS	-	-
26	TEST6	Connect to VSS	-	-
27	D00	Display Data Input (R) 00h for Black Display D20: LSB D25: MSB Driver IC carries out gamma conversion internally.	110	DR0
28	D01		111	DR1
29	D02		112	DR2
30	D03		114	DR3
31	D04		115	DR4
32	D05		116	DR5
33	VSS	GND	-	-
34	RL	Right/Left Display Reverse (Low: Normal Display, High: Reverse Display)	-	-
35	VDD	Power Supply	-	-
36	VDD	Power Supply	-	-
37	DISP	Display Control Signal (Low: Display OFF, High: Display ON)	-	-
38	DE	Input Data Effective Signal (Positive Polarity)	136	BLANK_N
39	UD	Up/Down Reverse	-	-

		(Low: Normal Display, High: Reverse Display)		
40	VSS	GND	-	-
41	VBL	Power Supply for Backlight	-	-
42	VBL	Power Supply for Backlight	-	-
43	PDM	Brightness Control Pulse Signal (Low: 0% (Backlight OFF) Brightness High: 100%)	-	-
44	VSS	GND	-	-
45	VSS	GND	-	-

Notice) The followings are the pins for VSS of VC1D.

Pin No.: 8, 19, 28, 32, 43, 51, 62, 72, 82, 93, 103, 113, 123, 134

3.2.2. Connection Diagram



※ The value of the dumping resistors needs to be adjusted to actual layout pattern.

3.2.3. Example of Register Settings

The following is an example of the register settings for VGA and these settings needs to be modified according to customers' design.

- VGA（640×480）mode

R#04h: INTL	0	(0h)
R#04h: CSYPAL	0	(0h)
R#04h: CSYOE	0	(0h)
R#04h: REVSY	0	(0h)
R#04h－R#05h: VTL[9:0]	521	(209h)
R#06h－R#07h: HTL[10:0]	798	(31Eh)
R#08h－R#09h: VBLS[9:0]	515	(203h)
R#0Ah－R#0Bh: HBLS[10:0]	783	(30Fh)
R#0Ch－R#0Dh: VBLE[9:0]	35	(023h)
R#0Eh－R#0Fh: HBLE[10:0]	143	(08Fh)
R#10h－R#11h: VDS[9:0]	35	(023h)
R#12h－R#13h: HDS[10:0]	143	(08Fh)
R#14h－R#15h: VDE[9:0]	515	(203h)
R#16h－R#17h: HDE[10:0]	783	(30Fh)
R#18h: VSW[3:0]	2	(2h)
R#19: HSW[7:0]	30	(1Eh)

※ This is an example of the register settings when DOTCLK is 25.175NHz.

3.3. COM41T4148

This chapter explains how to connect VC1D to COM41T4148.

3.3.1. Pin Correspondence Table

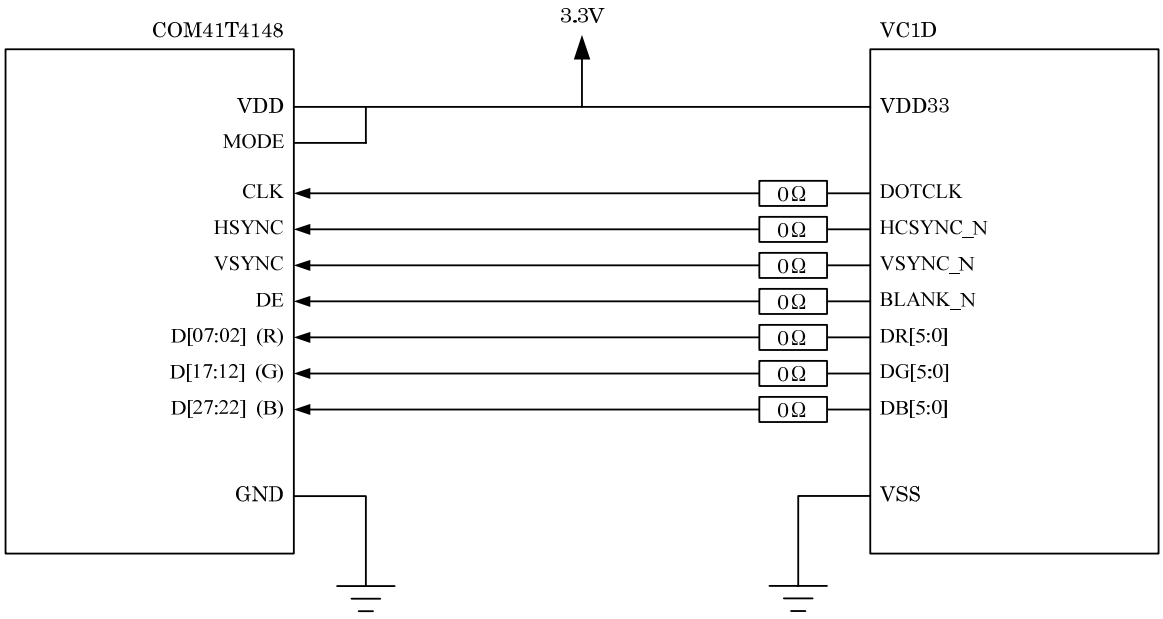
LCD Panel Connector Pin No.	LCD Panel Pin Name	LCD Panel Pin Description	VC1D Pin No.	VC1D Pin Name
1	VCOM	Common-Electrode Driving Signal	-	-
2	D27	Display Data Input (B) 00h for Black Display D22：LSB D27：MSB Driver IC carries out gamma conversion internally.	132	DB5
3	D26		131	DB4
4	D25		130	DB3
5	D24		128	DB2
6	D23		127	DB1
7	D22		125	DB0
8	D21	Connect to VSS	-	-
9	D20	Connect to VSS	-	-
10	D17	Display Data Input (G) 00h for Black Display D22：LSB D27：MSB Driver IC carries out gamma conversion internally.	124	DG5
11	D16		122	DG4
12	D15		121	DG3
13	D14		120	DG2
14	D13		119	DG1
15	D12		117	DG0
16	D11	Connect to VSS	-	-
17	D10	Connect to VSS	-	-
18	D07	Display Data Input (R) 00h for Black Display D22：LSB D27：MSB Driver IC carries out gamma conversion internally.	116	DR5
19	D06		115	DR4
20	D05		114	DR3
21	D04		112	DR2
22	D03		111	DR1
23	D02		110	DR0
24	D01	Connect to VSS	-	-
25	D00	Connect to VSS	-	-
26	BLON	OPEN	-	-
27	CS/STBY	STBY: Stand-by Control Signal (High Active)	-	-
28	DI/DE	DE: Input Data Effective Signal (High Active)	136	BLANK_N
29	SCK/REV	REV：Up/Down & Left/Right Display Reverse (Low：Normal Display, High：Reverse Display)	-	-
30	VSYNC	Vertical Synch. (Negative Polarity)	133	VSYNC_N
31	HSYNC	Horizontal Synch. (Negative Polarity)	135	HCSYNC_N
32	CLK	Dot Clock (Data Sampling at falling edge)	137	DOTCLK
33	VSS	GND	-	-
34	MODE	Mode Select ← Connect to VDD	-	-
35	POCB	Power On Clear (Low Active)	-	-
36	NC	OPEN	-	-
37	RVDD	Internal Power Supply	-	-
38	COMDC	Common-electrode Drive for DC Output	-	-
39	NC	OPEN	-	-
40	VSREF	Built-In DAC Reference Supply	-	-

41	C1P	Contacting Pin of Capacitor for Charge Pump	-	-
42	C1M	Contacting Pin of Capacitor for Charge Pump	-	-
43	C2M	Contacting Pin of Capacitor for Charge Pump	-	-
44	C2P	Contacting Pin of Capacitor for Charge Pump	-	-
45	VDD	Power Supply Input	-	-
46	COMOUT	Square Wave Output for Common-electrode	-	-
47	VDD2	Internal Power Supply	-	-
48	VSS	GND	-	-
49	VSS	GND	-	-
50	VSS	GND	-	-
51	C3M	Contacting Pin of Capacitor for Charge Pump	-	-
52	C3P	Contacting Pin of Capacitor for Charge Pump	-	-
53	C4M	Contacting Pin of Capacitor for Charge Pump	-	-
54	C4P	Contacting Pin of Capacitor for Charge Pump	-	-
55	VVCOM	Voltage Output for COMOUT	-	-
56	NC	OPEN	-	-
57	NC	OPEN	-	-
58	VGH	Positive Supply for Gate Driver	-	-
59	C5P	Contacting Pin of Capacitor for Charge Pump	-	-
60	C5M	Contacting Pin of Capacitor for Charge Pump	-	-
61	VGL	Negative Supply for Gate Driver	-	-
62	BLL2	LED Drive Source 2 (Cathode Side)	-	-
63	BLH2	LED Drive Source 2 (Anode Side)	-	-
64	NC	OPEN	-	-
65	NC	OPEN	-	-
66	BLH1	LED Drive Source 1 (Anode Side)	-	-
67	BLL1	LED Drive Source 1 (Cathode Side)	-	-

Notice) The followings are the pins for VSS of VC1D.

Pin No.: 8, 19, 28, 32, 43, 51, 62, 72, 82, 93, 103, 113, 123, 134

3.3.2. Connection Diagram



※ The value of the dumping resistors needs to be adjusted to actual layout pattern.

3.3.3. Example of Register Settings

The following is a example of the register settings for QVGA and these settings need to be modified according to customers' design.

- QVGA（320×240）Mode

R#04h: INTL	0	(0h)
R#04h: CSYPAL	0	(0h)
R#04h: CSYOE	0	(0h)
R#04h: REVSY	0	(0h)
R#04h－R#05h: VTL[9:0]	258	(102h)
R#06h－R#07h: HTL[10:0]	428	(1ACh)
R#08h－R#09h: VBLS[9:0]	260	(104h)
R#0Ah－R#0Bh: HBLS[10:0]	396	(18Ch)
R#0Ch－R#0Dh: VBLE[9:0]	20	(014h)
R#0Eh－R#0Fh: HBLE[10:0]	76	(04Ch)
R#10h－R#11h: VDS[9:0]	20	(014h)
R#12h－R#13h: HDS[10:0]	76	(04Ch)
R#14h－R#15h: VDE[9:0]	260	(104h)
R#16h－R#17h: HDE[10:0]	396	(18Ch)
R#18h: VSW[3:0]	2	(2h)
R#19: HSW[7:0]	10	(0Ah)

※ This is an example of the register settings when DOTCLK is 6.750MHz.

3.4. COM57T5135

This chapter explains how to connect VC1D to COM57T5135.

3.4.1. Pin Correspondence Table

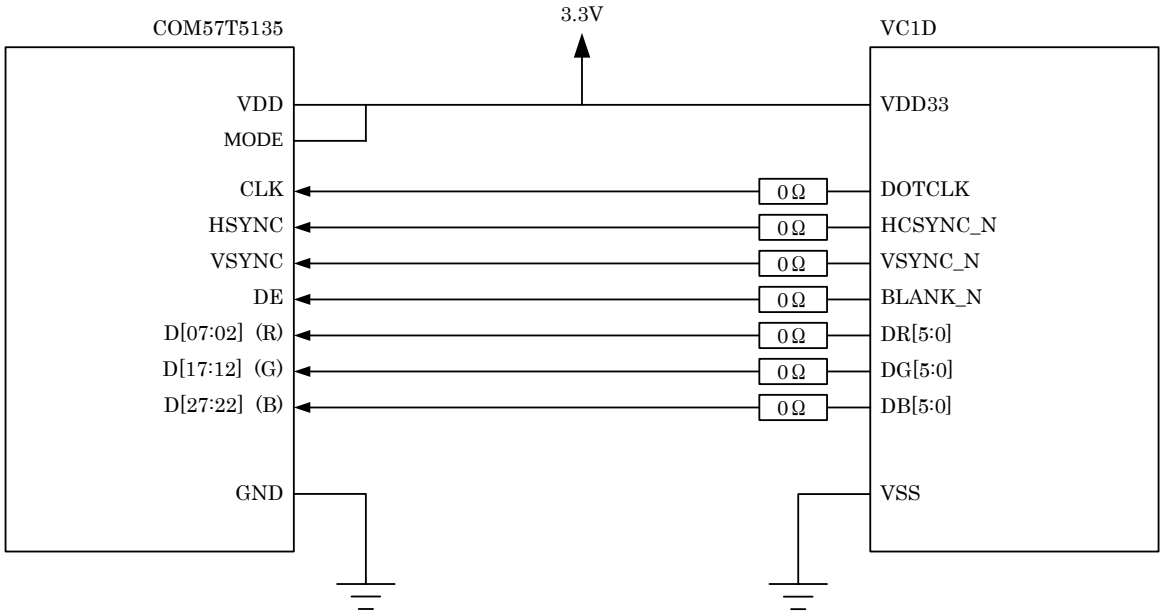
LCD Panel Connector Pin No.	LCD Panel Pin Name	LCD Panel Pin Description	VC1D Pin No.	VC1D Pin Name
1	VSS	GND	-	-
2	CLK	Dot Clock (Data Sampling at falling edge)	137	DOTCLK
3	VSS	GND	-	-
4	HSYNC	H-synch. (Negative Polarity)	135	HCSYNC_N
5	VSYNC	V-synch. (Negative Polarity)	133	VSYNC_N
6	VSS	GND	-	-
7	D20	Connect to VSS	-	-
8	D21	Connect to VSS	-	-
9	D22	Display Data Input (B) 00h for Black Display D22：LSB D27：MSB Driver IC carries out gamma conversion internally.	125	DB0
10	D23		127	DB1
11	D24		128	DB2
12	D25		130	DB3
13	D26		131	DB4
14	D27		132	DB5
15	VSS	GND	-	-
16	D10	Connect to VSS	-	-
17	D11	Connect to VSS	-	-
18	D12	Display Data Input (G) 00h for Black Display D22：LSB D27：MSB Driver IC carries out gamma conversion internally.	117	DG0
19	D13		119	DG1
20	D14		120	DG2
21	D15		121	DG3
22	D16		122	DG4
23	D17		124	DG5
24	VSS	GND	-	-
25	D00	Connect to VSS	-	-
26	D01	Connect to VSS	-	-
27	D02	Display Data Input (R) 00h for Black Display D22：LSB D27：MSB Driver IC carries out gamma conversion internally.	110	DR0
28	D03		111	DR1
29	D04		112	DR2
30	D05		114	DR3
31	D06		115	DR4
32	D07		116	DR5
33	VSS	GND	-	-
34	MODE	Mode Select ← Connect to VDD	-	-
35	VDD	Power Supply	-	-
36	VDD	Power Supply	-	-
37	CS/STBY	STBY：Stand-by Control Signal (High Active)	-	-
38	DI/DE	DE：Input Data Effective Signal (High Active)	136	BLANK_N
39	SCK/REV	REV：Up/Down & Left/Right Display Reverse (Low ：Normal Display, High：Reverse Display)	-	-
40	VSS	GND	-	-

41	VBL	Power Supply for Backlight	-	-
42	VBL	Power Supply for Backlight	-	-
43	PDM	Brightness Control Pulse Signal (Low：0%(Backlight Off) Brightness High：100%)	-	-
44	VSS	GND	-	-
45	VSS	GND	-	-

Notice）The following are the pins for VSS of　VC1D.

Pin No.: 8, 19, 28, 32, 43, 51, 62, 72, 82, 93, 103, 113, 123, 134

3.4.2. Connection Diagram



※ The value of the dumping resistors needs to be adjusted to actual layout pattern.

3.4.3. Example of Register Settings

The following is an example of the register settings for QVGA and these settings need to be modified to customers' design.

- QVGA（320×240）Mode

R#04h: INTL	0	(0h)
R#04h: CSYPAL	0	(0h)
R#04h: CSYOE	0	(0h)
R#04h: REVSY	0	(0h)
R#04h－R#05h: VTL[9:0]	258	(102h)
R#06h－R#07h: HTL[10:0]	428	(1ACh)
R#08h－R#09h: VBLS[9:0]	246	(0F6h)
R#0Ah－R#0Bh: HBLS[10:0]	362	(16Ah)
R#0Ch－R#0Dh: VBLE[9:0]	6	(006h)
R#0Eh－R#0Fh: HBLE[10:0]	42	(02Ah)
R#10h－R#11h: VDS[9:0]	6	(006h)
R#12h－R#13h: HDS[10:0]	42	(02Ah)
R#14h－R#15h: VDE[9:0]	246	(0F6h)
R#16h－R#17h: HDE[10:0]	362	(16Ah)
R#18h: VSW[3:0]	2	(2h)
R#19: HSW[7:0]	10	(0Ah)

※ This is an example of the register settings when DOTCLK is 6.750MHz.

3.5. COM35H3827

This chapter explains how to connect VC1D to COM35H3827.

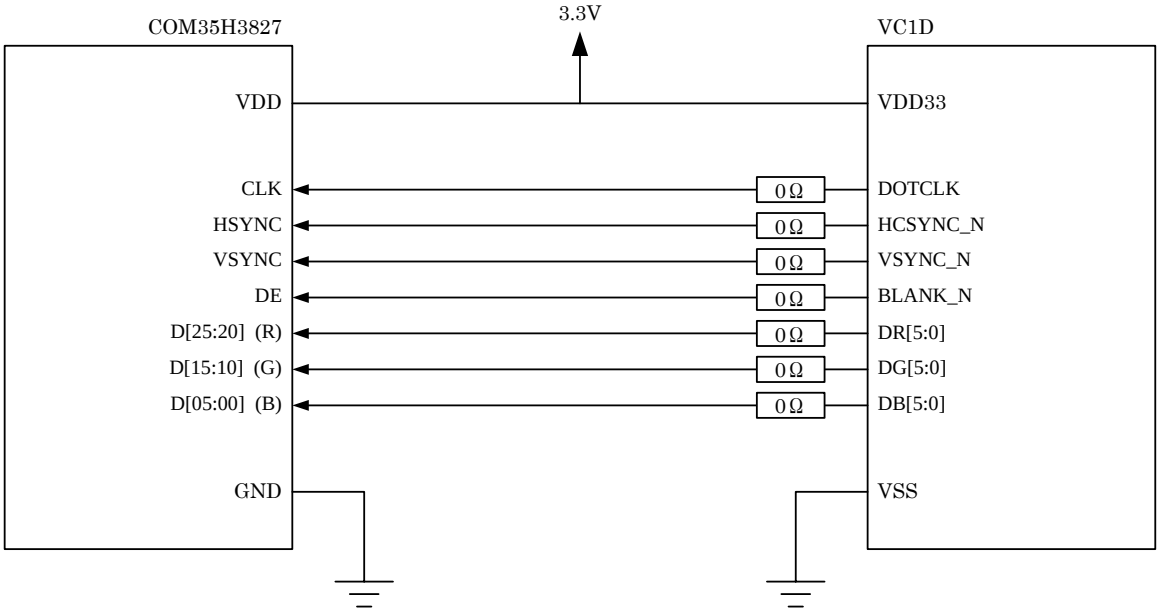
3.5.1. Pin Correspondence Table

LCD Panel Connector Pin No.	LCD Panel Pin Name	LCD Panel Pin Description	VC1D Pin No.	VC1D Pin Name
1	VSS	GND	-	-
2	VSS	GND	-	-
3	VDD	Power Supply	-	-
4	VDD	Power Supply	-	-
5	VSS	GND	-	-
6	RESETB	Reset Signal (Low Active)	-	-
7	HSYNC	Horizontal Synch. (Negative Polarity)	135	HCSYNC_N
8	VSYNC	Vertical Synch. (Negative Polarity)	133	VSYNC_N
9	CLK	Dot Clock (Data Sampling at falling edge)	137	DOTCLK
10	VSS	GND	-	-
11	D00	Display Data Input (B) 00h for Black Display D00：LSB D05：MSB Driver IC carries out gamma conversion internally.	125	DB0
12	D01		127	DB1
13	D02		128	DB2
14	D03		130	DB3
15	D04		131	DB4
16	D05		132	DB5
17	D10	Display Data Input (G) 00h for Black Display D00：LSB D05：MSB Driver IC carries out gamma conversion internally.	117	DG0
18	D11		119	DG1
19	D12		120	DG2
20	D13		121	DG3
21	D14		122	DG4
22	D15		124	DG5
23	D20	Display Data Input (R) 00h for Black Display D00：LSB D05：MSB Driver IC carries out gamma conversion internally.	110	DR0
24	D21		111	DR1
25	D22		112	DR2
26	D23		114	DR3
27	D24		115	DR4
28	D25		116	DR5
29	VSS	GND	-	-
30	DE	Input Data Effective Signal (High Active)	136	BLANK_N
31	STBYB	Stand-by Control Signal (Low：Stand-by Operation, High：Normal Operation)	-	-
32	TEST1	MODE1(Connect to GND)	-	-
33	NC	OPEN	-	-
34	NC	OPEN	-	-
35	NC	OPEN	-	-
36	NC	OPEN	-	-
37	TEST2	MODE2(Connect to GND)	-	-
38	BLH	LED Drive Source (Anode Side)	-	-
39	BLL	LED Drive Source (Cathode Side)	-	-

注）The followings are the pins for VSS of VC1D.

Pin No.: 8, 19, 28, 32, 43, 51, 62, 72, 82, 93, 103, 113, 123, 134

3.5.2. Connection Diagram



※ The value of the dumping resistors needs to be adjusted according to actual layout pattern.

3.5.3. Example of Register Settings

The following is an example of the register settings for QVGA and these settings need to be modified to customers' design.

- QVGA（240×320）Mode

R#04h: INTL	0	(0h)
R#04h: CSYPAL	0	(0h)
R#04h: CSYOE	0	(0h)
R#04h: REVSY	0	(0h)
R#04h－R#05h: VTL[9:0]	321	(141h)
R#06h－R#07h: HTL[10:0]	286	(11Eh)
R#08h－R#09h: VBLS[9:0]	323	(143h)
R#0Ah－R#0Bh: HBLS[10:0]	249	(0F9h)
R#0Ch－R#0Dh: VBLE[9:0]	3	(003h)
R#0Eh－R#0Fh: HBLE[10:0]	9	(009h)
R#10h－R#11h: VDS[9:0]	3	(003h)
R#12h－R#13h: HDS[10:0]	9	(009h)
R#14h－R#15h: VDE[9:0]	323	(143h)
R#16h－R#17h: HDE[10:0]	249	(0F9h)
R#18h: VSW[3:0]	0	(0h)
R#19: HSW[7:0]	1	(01h)

※ This is an example of the register settings when DOTCLK is 5.600MHz.

Revision History

Date	Rev.	内容
2009/11/13	1.0.6	1st Release
2009/11/19	1.0.7	“List of Casio LCD panels supported by VC1D” in the chapter 2 updated
2010/11/8	1.0.8	“Casio” -> “ORTUS TECHNOLOGY” File name was changed.
2010/12/10	1.0.9	“COM57T5137” -> “COM57H5137” “COM57H5M08” -> “COM57T5M08” “COM41T4156” -> “COM41H4156” Information of “COM50T5119” and “COM50T5117” were deleted. “COM50T5125” -> “COM50H5125” “COM57H5M04” -> “COM57T5M04”
2011/5/30	1.1.0	1. Outline: The link information was changed.

AGENT

YAMAHA CORPORATION

Address inquiries to:
Semiconductor Sales & Marketing Department

■ Head Office 203, Matsunokijima, Iwata,
Shizuoka, 438-0192, Japan
Tel. +81-539-62-4918 Fax. +81-539-62-5054

■ Tokyo Office 2-17-11, Takanawa, Minato-ku,
Tokyo, 108-8568, Japan
Tel. +81-3-5488-5431 Fax. +81-3-5488-5088

■ Osaka Office 3-12-12, Minami Senba, Chuo-ku,
Osaka City, Osaka, 542-0081, Japan
Tel. +81-6-6252-6221 Fax. +81-6-6252-6229

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