YAMAHA

YGV632

VC1D

Video Controller 1 with Video Decoder

■ Overview

YGV632 (“VC1D” is a function name) is the display controller which makes it easier to create a highly colorful graphic image in a low-cost system configuration.

With a built-in digital video recorder, it is easy to build up a system of superimposing characters, lines or graphic icons (up to 65536 color expression) over CVBS signals (Composite Video Signals) from a CCD camera, etc. Although there is an LSI called OSDC (OSD controller), which are occasionally used as a low-cost system for superimposing characters and simple graphics over video signals, YGV632 realizes impressively higher colorful picture expression under an equivalent control load to OSDC. Particularly, since the sprite system is used for generating graphic planes, it is possible to represent moving images like animation even in CPU control by serial port communication.

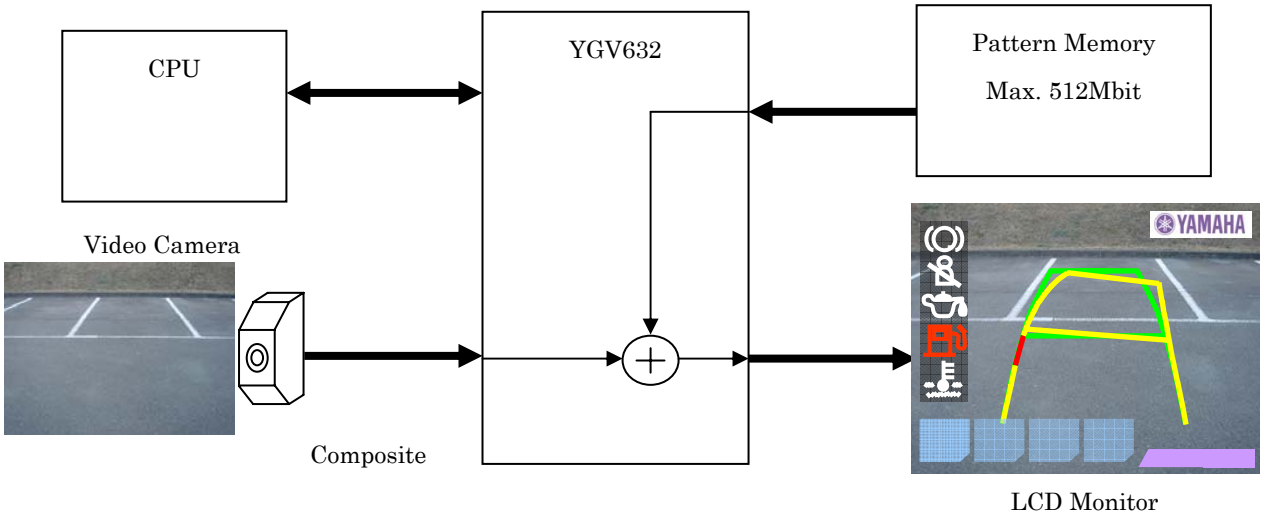
A pattern memory for storing bitmap picture data called “sprites” or font data is externally connectable to YGV632 (up to 512 Mbits). For using a sprite data, the CPU just needs to specify a sprite stored beforehand in the patter memory by its pattern memory address and specify the position coordinates of the sprite on the display plane; then, YGV632 automatically loads the sprite data from the pattern memory so as to superimpose it over input video for output.

YGV632 does not need such cumbersome frame memory management as existing graphic controllers do, which contributes to reducing man-hours for development of control programs.

YAMAHA CORPORATION

YGV632 CATALOG
CATALOG No.: LSI-4GV632A50
2011.5

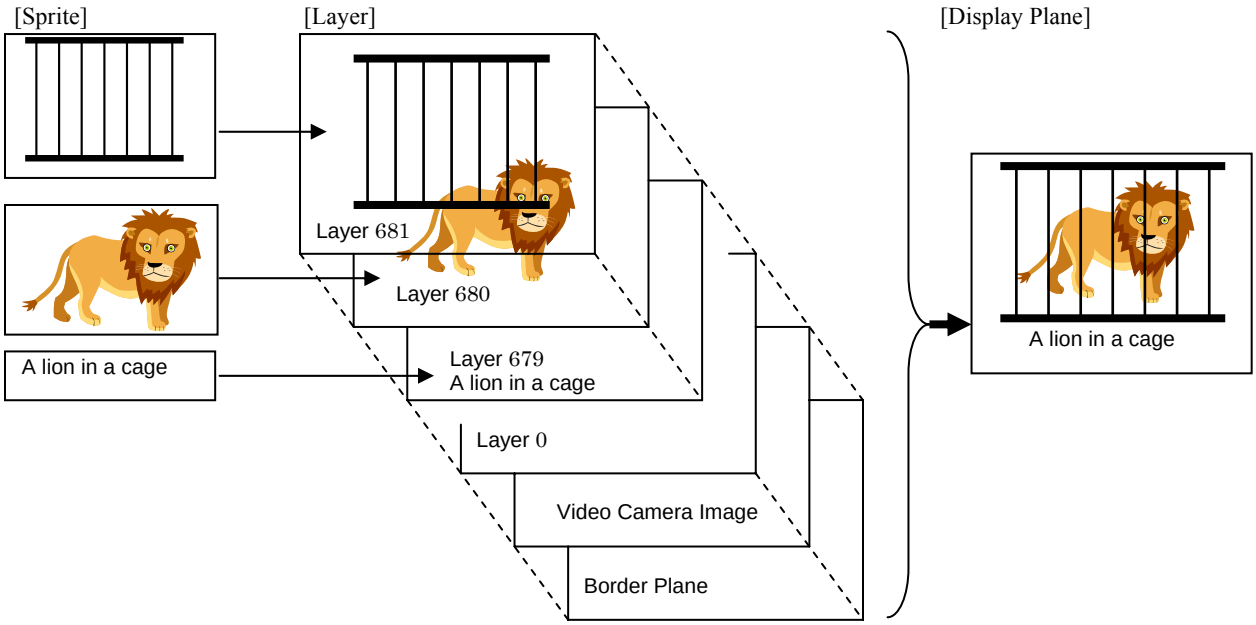
YGV632 contains a VRAM (line buffer). This is why a system configuration using less part becomes possible.



With recent increasing safety consciousness, automobiles equipped with a video camera can be frequently seen, one of which is a system that superimposes lines, etc. indicating the car-width onto a camera image to help one's operation required for parking.

YGV632 has a function that draws a line freely onto a camera image and it meets the temperature guarantee conditions for in-car product. YGV632 is best suited for ECU with an in-car camera.

YGV632 can superimpose up to 682 images onto one video.



■ Features

☐ Display function
- ➢ Monitor supported
  - TFT liquid crystal display (digital RGB connection [i]) or a display equipment with the equivalent I/F
- ➢ Monitor resolution
  - Programmable for NTSC, PAL, QVGA, Wide QVGA, VGA, Wide VGA, SVGA
- ➢ Display plane functions
  - Capable of display of text, video footage, lines by free drawing, and pattern data by sprite system
  - Layered structure up to 682 layers and up to one capture plane layer
  - Displays sprites, lines and texts by layers
  - Alpha-blending control by the pixel (alpha by pixel)
  - Layer picture quality adjustment function (contrast, brightness)

☐ Graphic generation function
- ➢ Sprite
  - Sprite display: up to 682 per field
  - Size: 8x8 to 512x512 dots, horizontal and vertical scaling values independently selectable (by 8 dots)
  - 2, 16, 32, 64, or 256 palette colors in 64k colors, 65536-color natural picture display by 16-bit RGB
  - Flip vertical and horizontal
  - Scaling function
  - Alpha-blending in pixels
  - Anti-aliasing function in the outline part
- ➢ Text
  - Specifies a font type per character string
  - Supports variable-width fonts such as proportional fonts
  - Scaling function
  - Supports fonts for anti-aliasing
- ➢ Line drawing
  - Direct drawing by specification of start/end point coordinates (pattern data is not needed)
  - Line display is settable up to 1022 lines in a field
  - Display color: 32768-color (RGB555) specification or palette index (10 bits) specification
  - Line width: 1 dot to 16 dots assignable (by the dot)
  - Anti-aliasing drawing function

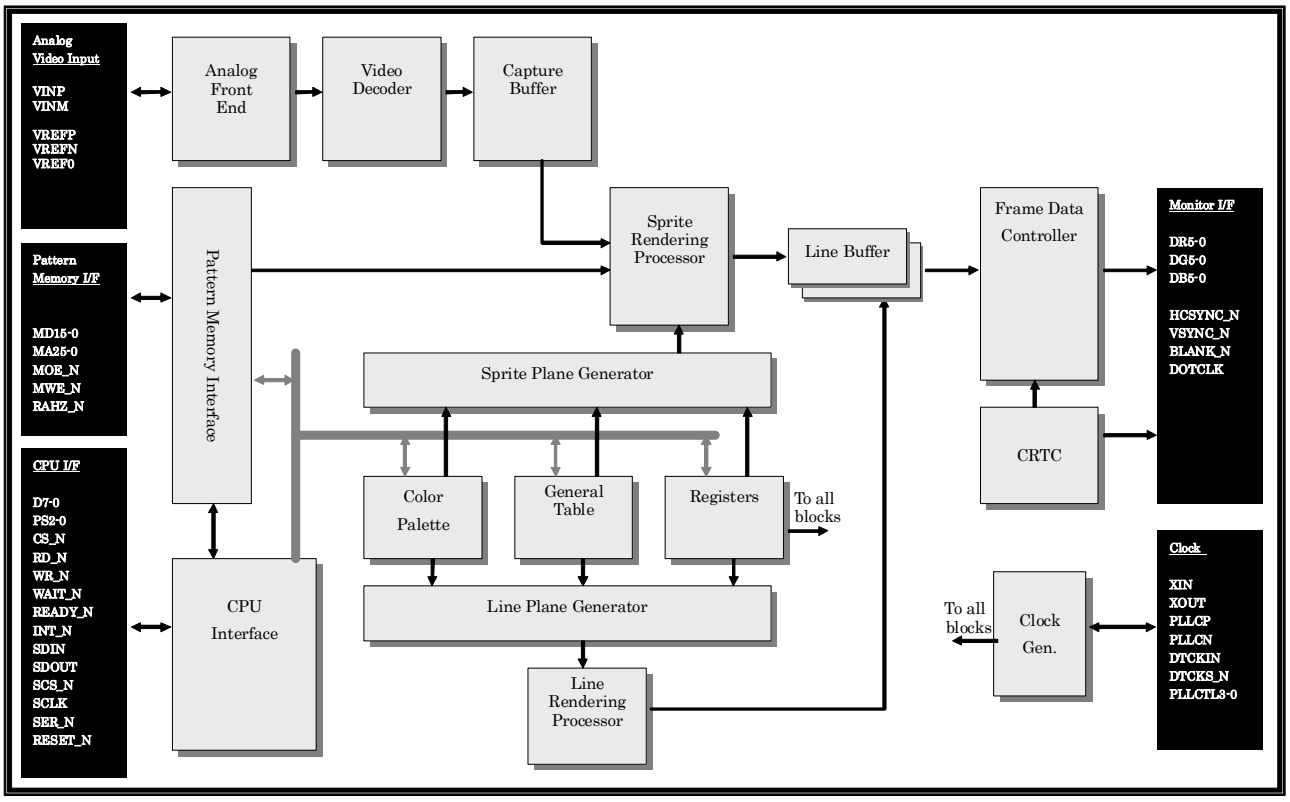
☐ Video footage input and capture
- ➢ Built-in digital video decoder
  - Inputs directly composite video signals in NTSC/PAL and then converts them to digital RGB
  - Contrast, brightness, color saturation and hue adjustment function
  - Color killer function, video input detection function
- ➢ Built-in capture buffer
  - Capable of stable video output when input video has synchronizing disturbance (TBC function)
  - Slope correction of capture video
  - Distortion correction of capture video
  - Mirror inversion function of capture video
  - Usable as a wallpaper frame buffer when no input video is present

[i] For use of an analog RGB monitor, use DAC or YGV629, a sister product.

☐ Others

- ➢ CPU interface
  - 8-bit parallel or serial connection
  - Indirect mapping to the built-in registers and tables through the access ports
- ➢ Pattern memory interface
  - Up to 512 Mbits, 8-bit/16-bit bus width
  - Mask ROM [i], SRAM, and NOR type flash-memory connectable
  - Access timing can be set by the system clock cycle
- ➢ Device specifications
  - Lead-free 144-pin LQFP package (YGV632-VZ)
  - Supply voltage: 3.3V (regulator for core voltage is built in)
  - CPU interface power supply variable between 3.3V and 5V
  - Operation temperature range from -40°C to +85°C

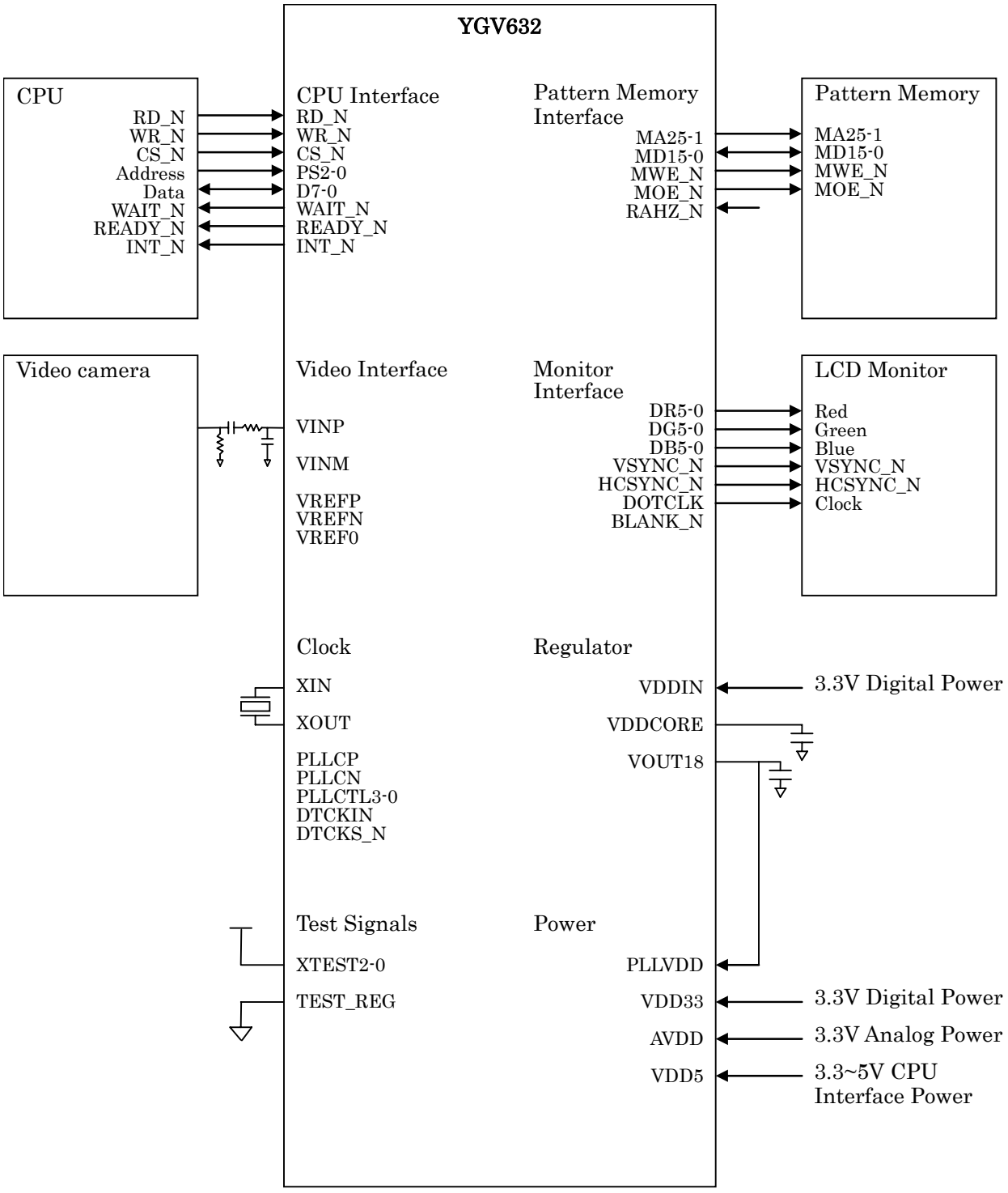
■ Block Diagram



[i] Timing-compatible ROM (OTPROM, EPROM, etc.) can be also connected.

■ Example of System Configuration

A system configuration using YGV632 is shown below.



■ Pin Table

CPU Interface

Pin Name	Num.	I/O	Attrib.	Function	CPU connection	Power	Level	Drive
D7-0	8	I/O	—	CPU data bus	5V I/F(O) 5V tolerant(I)	VDD5	CMOS	4mA
PS2-0	3	I	—	CPU port selection	5V tolerant	VDD33	CMOS	
CS_N	1	I	—	Chip select (dual-purpose pin)	5V tolerant	VDD33	CMOS	
RD_N	1	I	—	Read pulse (dual-purpose pin)	5V tolerant	VDD33	CMOS	
WR_N	1	I	—	Write pulse (dual-purpose pin)	5V tolerant	VDD33	CMOS	
WAIT_N	1	O	OT	CPU bus wait (3-state output) (dual-purpose pin)	5V I/F	VDD5	CMOS	4mA
READY_N	1	O	OT	CPU bus ready (3-state output)	5V I/F	VDD5	CMOS	4mA
INT_N	1	O	OD	Interrupt (open drain)	5V I/F	VDD5	CMOS	4mA
SER_N	1	I	—	CPU interface selection	—	VDD33	CMOS	
SCS_N	1	I	—	Serial interface chip select (dual-purpose pin)	5V tolerant	VDD33	CMOS	
SDIN	1	I	—	Serial interface data input (dual-purpose pin)	5V tolerant	VDD33	CMOS	
SDOUT	1	O	OT	Serial interface data output (3-state output) (dual-purpose pin)	5V I/F	VDD5	CMOS	4mA
SCLK	1	I	—	Serial clock input (dual-purpose pin)	5V tolerant	VDD33	CMOS	
RESET_N	1	I	I$	Reset	5V tolerant	VDD33	CMOS	

PATTERN MEMORY Interface

Pin Name	Num.	I/O	Attrib.	Function	Power	Level	Drive
MD15-0	16	I/O	—	Pattern memory data bus	VDD33	LVCMOS	4mA
MA25-0	26	O	OT	Pattern memory address bus (3-state output)	VDD33	LVCMOS	4mA
MOE_N	1	O	OT	Pattern memory output enable (3-state output)	VDD33	LVCMOS	4mA
MWE_N	1	O	OT	Pattern memory write pulse (3-state output)	VDD33	LVCMOS	4mA
RAHZ_N	1	I	—	Pattern memory high impedance switching	VDD33	LVCMOS	

Video Interface

Pin Name	Num.	I/O	Attrib.	Function	Power	Level	Drive
VINP	1	I	A	Analog video input	AVDD	Analog	
VINM	1	I	A	Input pin for test	AVDD	Analog	
VREF0	1	IO	A	ADC reference pin	AVDD	Analog	
VREFP	1	IO	A	Plus reference voltage pin for ADC	AVDD	Analog	
VREFN	1	IO	A	Minus reference voltage pin for ADC	AVDD	Analog	

Monitor Interface

Pin Name	Num.	I/O	Attrib.	Function	Power	Level	Drive
DR5-0	6	O	—	Digital video: Red output	VDD33	LVCMOS	2mA
DG5-0	6	O	—	Digital video: Green output	VDD33	LVCMOS	2mA
DB5-0	6	O	—	Digital video: Blue output	VDD33	LVCMOS	2mA
VSYNC_N	1	O	—	Vertical synchronizing signal output	VDD33	LVCMOS	2mA
HCSYNC_N	1	O	—	Horizontal synchronizing signal or composite synchronizing signal output	VDD33	LVCMOS	2mA
BLANK_N	1	O	—	Display timing output	VDD33	LVCMOS	2mA
DOTCLK	1	O	—	Dot clock output	VDD33	LVCMOS	2mA

Clock

Pin Name	Num.	I/O	Attrib.	Function	Power	Level	Drive
XIN	1	I	—	Reference clock input	VDD33		
XOUT	1	O	—	Crystal connection pin	VDD33		
DTCKIN	1	I	—	Dot clock input pin	VDD33	LVCMOS	
DTCKS_N	1	I	—	Dot clock input select pin	VDD33	LVCMOS	
PLLCTL3-0	4	I	—	PLL frequency dividing proportion setting pin	VDD33	LVCMOS	
PLLCP	1	—	A	PLL filter connection pin, Plus side	PLLVDD	Analog	
PLLCN	1	—	A	PLL filter connection pin, GND side	PLLVDD	Analog	

For device

Pin Name	Num.	I/O	Attrib.	Function	CPU connection	Power	Level	Drive
XTEST2-0	3	I	—	Test pin	—	VDD33	LVCMOS	
VDD33	11	—	—	Digital power supply 3.3V	—	—		
VDD5	1	—	—	Power supply for CPU interface (3.3 to 5V)	—	—		
VSS	14	—	—	Digital VSS	—	—		
PLLVDD	1	—	—	Power supply for PLL	—	—		
AVDD	1	—	—	Power supply for Analog Front End	—	—		
AVSS	1	—	—	VSS for Analog Front End	—	—		
OCPEN	1	I	—	Reset of excess current protection circuit ("L" input) Switch between use and stop of excess current protection circuit	5V I/F	VDD5	CMOS	
TEST_REG	1	I	—	Operation/Stop control of excess current protection circuit	5V I/F	VDD5	CMOS	
OCP_N	1	O	—	Output of excess current detection state	—	VDD5	CMOS	4mA
VDDCORE	3	—	—	Capacitor connection pin for core power supply	—	VDDIN		
VOUT18	1	—	—	Digital power supply 1.8V output	—	VDDIN		
VDDIN	2	—	—	3.3V input for core power supply (1.8V)	—	—		

Total number of pins: 144 (148 pins minus 4 dual-purpose pins)

Note) YGV632 has no pull-up resistors built in it. Pull up the pins externally as necessary.

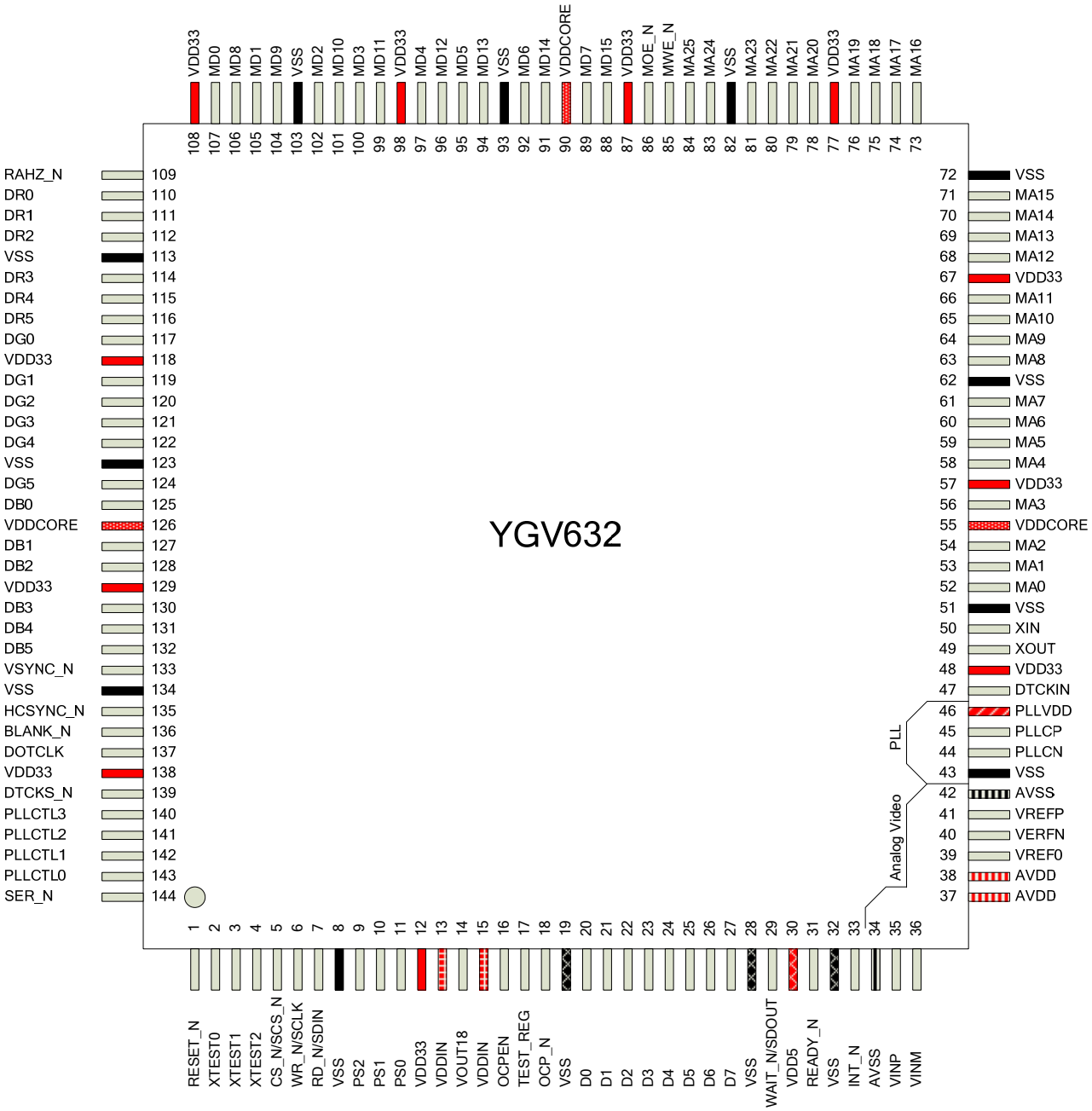
RE: The meanings of signs in several columns of the above tables are as follows.

[I/O]: I → input; O → output; I/O → input and output

[Attrib.]: I$ → schmitt trigger input; A → analog terminal; OD → open drain output; OT → 3-state output

As to the pins with “5V I/F” in the column of “CPU connection,” the voltage applied should be kept below VDD5 (power supply pin) + 0.5V.

■ Pin Arrangement Diagram



< 144-pin Top View >

■Electrical Characteristics

• Absolute Maximum Ratings

Items	Symbol	Rating	Unit	Note
Power Supply Voltage (VDD5 pin)	V_{DD5}	- 0.5 to +5.5	V	1
Power Supply Voltage (VDD33, VDDIN pin)	V_{DD33}	- 0.5 to +4.6	V	1
Analog Power Supply Voltage (AVDD pin)	V_{AVD}	- 0.5 to +4.6	V	1
PLL Power Supply Voltage (PLLVDD pin)	V_{PLVD}	- 0.5 to +2.0	V	1
Input Pin Voltage (5V tolerant pins)	V_I	- 0.5 to +5.5	V	1
Input Pin Voltage (VDD5 input pins)	V_I	- 0.5 to VDD5+0.5(≤ 5.5 Max)	V	1
Input Pin Voltage (Other input pins)	V_I	- 0.5 to VDD33+0.5(≤ 4.6 Max)	V	1
Output Pin Voltage (VDD5 output pins)	V_O	- 0.5 to +5.5	V	1
Output Pin Voltage (Other output pins)	V_O	- 0.5 to VDD33+0.5(≤ 4.6 Max)	V	1
Input Pin Current	I_I	- 20 to +20	mA	
Output Pin Current	I_O	- 20 to +20	mA	
Storage Temperature	T_{stg}	- 50 to +125	°C	

Note 1) Voltage relative to V_{SS}=0V.

• Recommended Operating Conditions

Items	Symbol	Min.	Typ.	Max.	Unit	Note
Power Supply Voltage (VDD33, VDDIN pin)	V_{DD33}	3.0	3.3	3.6	V	1
Analog Power Supply Voltage (AVDD pin)	V_{AVD}	3.0	3.3	3.6	V	1
PLL Power Supply Voltage (PLLVDD pin)	V_{PLVD}	1.65	1.8	1.95	V	1,2
CPU I/F Power Supply Voltage (VDD5 pin)	V_{DD5}	3.0	5.0	5.25	V	1
Operating Ambient Temperature	T_{OP}	- 40		85	°C	3

Note 1) Voltage relative to V_{SS}=0V.

Note 2) The PLLVDD pin is connected to the VOUT18 pin of this LSI.
It is not needed to have 1.8V power supply outside LSI.

Note 3) The board wiring density is estimated to be 200% or more.

• Consumption Current

Items	Conditions	Symbol	Min.	Typ.	Max.	Unit	Note
Total Power Consumption	C_L=20pF V_{IL}=GND V_{IH}=V_{DD33}	P_D			742	mW	1
Consumption Current Breakdown							
VDD33, VDDIN		I_{VDD}			150	mA	1,2
VDD5		I_{VDD5}			7.5	mA	1
AVDD		I_{AVD}			45	mA	1
PLLVDD		I_{PVD}			(5)	mA	1,2

Note 1) Consumption current value and power consumption value are the values under the recommended operating condition.

Note 2) The current value of "VDD33, VDDIN" includes the current flowing through PLLVDD pin because the internal regulator generates I_{PVD} current.

• DC Characteristics

Items	Symbol	Min.	Typ.	Max.	Unit	Note
Low Level Input Voltage (XIN pin)	V_{IL}	- 0.3		$0.3 \times V_{DD33}$	V	1
Low Level Input Voltage (Except the XIN pin)	V_{IL}	- 0.3		0.8	V	1
High Level Input Voltage (XIN pin)	V_{IH}	$0.7 \times V_{DD33}$		$V_{DD33} + 0.3$	V	1
High Level Input Voltage (Except XIN pin, except 5V tolerant input pin, 3.3V power supply)	V_{IH}	2.0		$V_{DD33} + 0.3$	V	1
High Level Input Voltage (5V tolerant input pin, 3.3V power supply: CS_N/SCS_N, WR_N/SCLK, RD_N/SDIN, PS2-0, RESET_N)	V_{IH}	2.0		5.5	V	1
High Level Input Voltage (D7-0)	V_{IH}	2.0		5.5	V	1
High Level Input Voltage (OCPEN, TEST_REG)	V_{IH}	2.0		$V_{DD5} + 0.3$	V	1

Note 1) Voltage relative to V_{SS}=0V.

Items	Conditions	Symbol	Min.	Typ.	Max.	Unit	Note
Low Level Output Voltage (Except XOUT pin, 3.3V power supply)	I_{OL}=100µA	V_{OL}	0		0.2	V	1
	I_{OL}=2mA	V_{OL}	0		0.4	V	1
Low Level Output Voltage (Except XOUT pin, 5V power supply)	I_{OL}=100µA	V_{OL}	0		0.2	V	1
	I_{OL}=4mA	V_{OL}	0		0.4	V	1
High Level Output Voltage (Except XOUT pin, 3.3V power supply)	I_{OH}= - 100µA	V_{OH}	V_{DD33} - 0.2		V_{DD33}	V	1
	I_{OH}= - 2mA	V_{OH}	2.4		V_{DD33}	V	1
Low Level Output Voltage (Except XOUT pin , 5V power supply)	I_{OH}= - 100µA	V_{OH}	V_{DD5} - 0.2		V_{DD5}	V	1
	I_{OH}= - 4mA	V_{OH}	$V_{DD5} \times 0.8$		V_{DD5}	V	1
Input Leak Current		I_{LI}	- 10		+ 10	µA	
Output Leak Current		I_{LO}	- 25		+ 25	µA	

Note 1) Voltage relative to V_{SS}=0V.

Items	Symbol	Min.	Typ.	Max.	Unit
Input Pin Capacitance	C_I			10	pF
Output Pin Capacitance	C_O			10	pF
Input-Output Pin Capacitance	C_{IO}			10	pF

Items	Symbol	Min.	Typ.	Max.	Unit	Note
Analog Video Input Voltage (VINP pin)	V_{VINP}		1.25	1.4	Vp-p	1

Note 1) The above maximum value is for the setting of "R#26: ADCGAIN=2'b00."

• AC Characteristics

Measurement Conditions

Input Voltage: 0V / V_{DD33}

Input transition time: 1ns (transition time is regulated between $V_{DD33} \times 0.2$ and $V_{DD33} \times 0.8$)

Measurement reference voltage: Input V_{IL}/V_{IH}

Output $V_{DD33}/2V$

Output load capacitance: 20pF

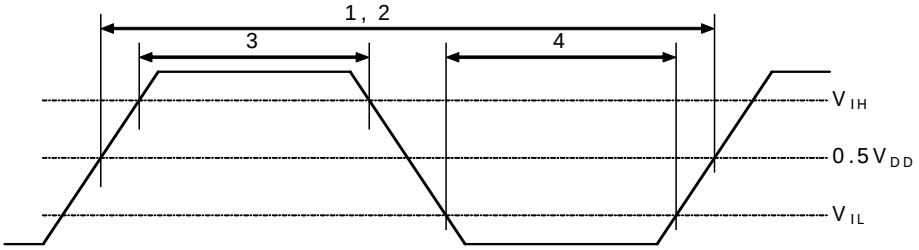
・Clock Input

No.	Items	Symbol	Min.	Typ.	Max.	Unit	Note
1	XIN Clock Frequency	f_{XIN}	6		40	MHz	
	XIN Clock Cycle Time	t_{XIN}	25		166	ns	
2	DTCKIN Clock Frequency	f_{DTCKIN}			40	MHz	
	DTCKIN Clock Cycle Time	t_{DTCKIN}	25			ns	
3	XIN, DTCKIN Clock High Level Pulse Width	t_{whCLK}	7.5			ns	
4	XIN, DTCKIN Clock Low Level Pulse Width	t_{wlCLK}	7.5			ns	
5	SYCLK Clock Frequency	f_{SYCLK}			83.16	MHz	1
	SYCLK Clock Cycle Time	t_{SYCLK}	12.03			ns	1
6	PLL Out Clock Frequency	f_{PLLO}	120		166.32	MHz	1
	PLL Out Clock Cycle Time	t_{PLLO}	6.01			ns	1
7	DCLK Clock Frequency	f_{DCLK}			40	MHz	2
	DCLK Clock Cycle Time	t_{DCLK}	25			ns	2

Note 1) SYCLK is an internal clock of 1/2 frequency division of PLL generation clock. t_{SYCLK} is derived from the below calculation formula with the XIN input clock(t_{XIN}).

$t_{SYCLK} = t_{XIN} \times k / 2n \quad (1 \leq k \leq 8, 1 \leq n \leq 32)$

Note 2) DCLK is a dot clock that is used internally.



・Power Supply and Reset Input

No.	Items	Symbol	Min.	Typ.	Max.	Unit	Note
1	RESET_N pin Input Time	t_{wRES}	10			µs	1
2	CPU Access Stand-by Time after RESET_N Negation	t_{wAW}	10 to 67			ms	
3	RESET_N Setup Time	t_{sRES}	0			ns	2
4	Power-on Time Difference (VDD33, VDDIN, AVDD)	t_{VSKWR}			1	s	3
5	Power-off Time Difference (VDD33, VDDIN, AVDD)	t_{VSKWF}			1	s	4
6	Power Rise Time	t_{VRISE}			200	ms	
7	VDD5 Power-on/off Time Difference	t_{VSKWC}	-1			s	5
8	Core Power VOUT18 Rise Time	t_{vCORE}			300	µs	6
9	OCPEN pin Input Time (Initialization)	t_{wOCPE}	10			µs	
10	OCPEN pin Low Input Time (Abnormal)	t_{wOCPR}	0.4		10	ms	

Note 1) The time from a point where a power supply powered up last reaches at 3.0V, VOUT18 reaches at 1.7V, and the input clock to the XIN pin becomes stable.

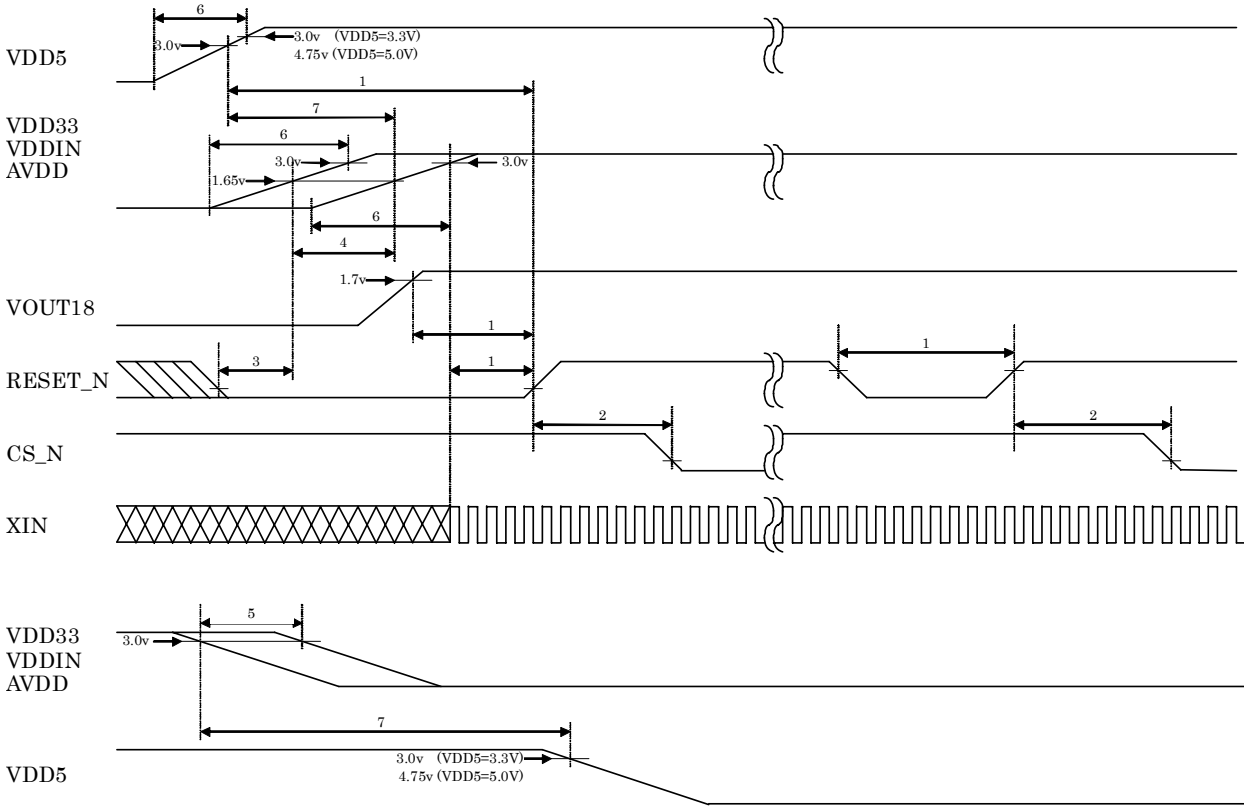
Note 2) This is the specification for a power supply powered up first out of VDD33, VDDIN, and AVDD.

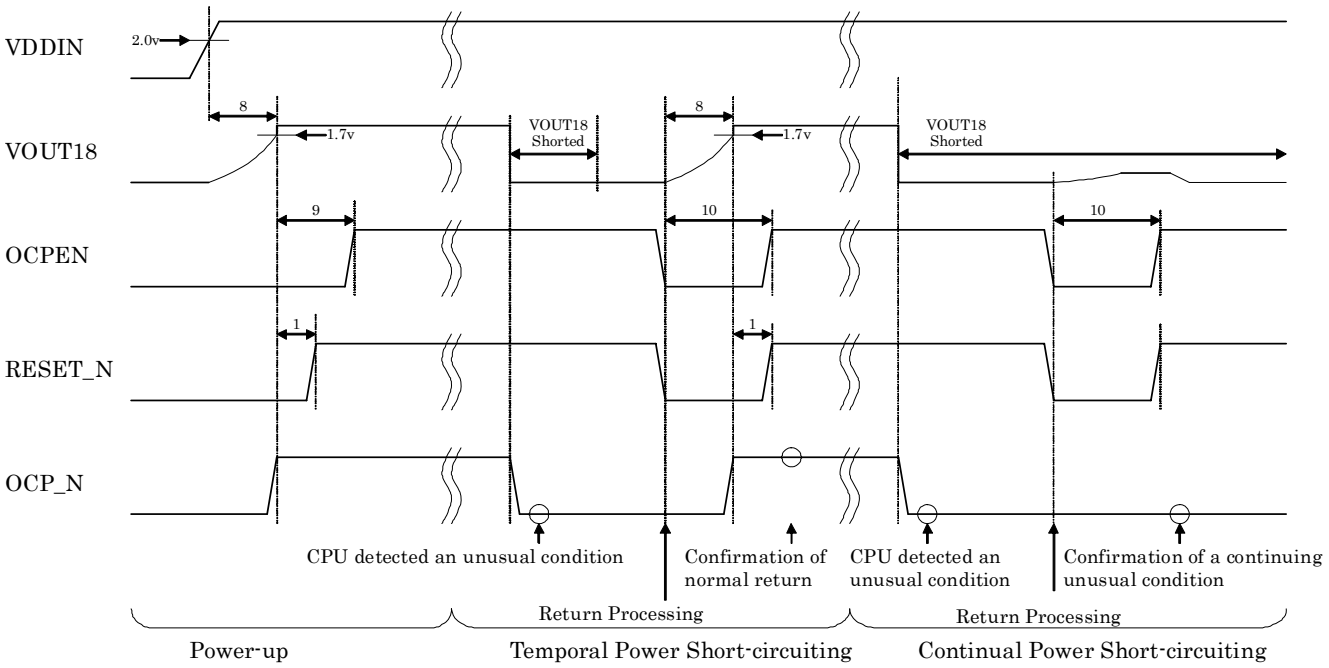
Note 3) It is recommended VDD33, VDDIN, and AVDD be turned on simultaneously. If 1 second or more time-difference occurs among their powering-on, it may affect the LSI's reliability.

Note 4) It is recommended VDD33, VDDIN, and AVDD be turned off simultaneously. If 1 second or more time-difference occurs among their powering-off, it may affect the LSI's reliability.

Note 5) It is possible to shutdown 3V power supply (VDD33, VDDIN, and AVDD) with 5V power (VDD5) applied.

Note 6) This is the value with four capacitors of 4.7µF connected to VOUT18 and VDDCORE pins.


VDD5
VDD33
VDDIN
AVDD
VOUT18
RESET_N
CS_N
XIN
3.0v (VDD5=3.3V)
4.75v (VDD5=5.0V)
1.65v
1.7v
VDD33
VDDIN
AVDD
VDD5
3.0v (VDD5=3.3V)
4.75v (VDD5=5.0V)


VDDIN
VOUT18
OCPEN
RESET_N
OCP_N
2.0v
1.7v
VOUT18
Shorted
CPU detected an unusual condition
Confirmation of
normal return
CPU detected an
unusual condition
Confirmation of a continuing
unusual condition
Return Processing
Return Processing
Power-up
Temporal Power Short-circuiting
Continual Power Short-circuiting

・CPU Interface

・Parallel Interface

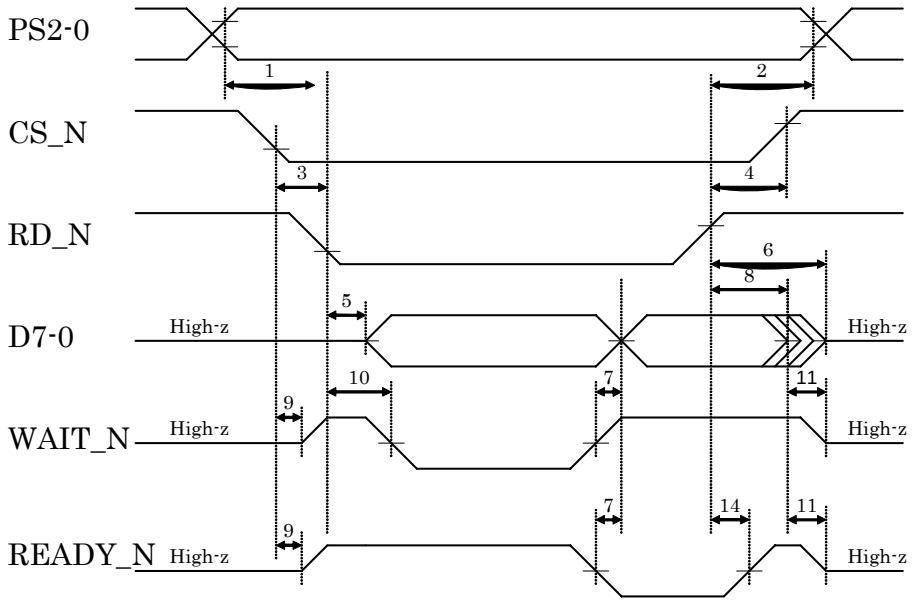
No.	Items	Symbol	Min.	Typ.	Max.	Unit	Note
1	PS2-0: Setup Time	t_{sA}	4			ns	1
2	PS2-0: Hold Time	t_{hA}	0				1
3	CS_N: Setup Time	t_{sCS}	0				2
4	CS_N: Hold Time	t_{hCS}	0				2
5	D7-0: Output Data Turn On Time	t_{onD}	0				
6	D7-0: Output Data Turn Off Time	t_{offD}			30		
7	D7-0: Output Data Enabled Delay Time	t_{dD}			0		
8	D7-0: Output Data Hold Time	t_{hD}	0				
9	WAIT_N, READY_N: Turn On Time	t_{onWAIT}	0				
10	WAIT_N, READY_N: Enabled Delay Time	t_{dWAIT}			25		
11	WAIT_N, READY_N: Turn Off Time	$t_{offWAIT}$			30		
12	D7-0: Input Data Setup Time	t_{sD}	t_{SYCLK}+15				
13	D7-0: Input Data Hold Time	t_{hD}	0				
14	READY_N: Hold Time	t_{hREADY}	0		30		
15	Command Pulse Active Time	t_{aCMD}	$2\times t_{SYCLK}$				3
16	Command Pulse Inhibit Time	t_{iCMD}	$4\times t_{SYCLK}$				3
17	Command Cycle Time	t_{cCMD}	$6\times t_{SYCLK}$				3

Note 1) Specifications for the WR_N and RD_N signals. However, at CS_N control, they are for CS_N.

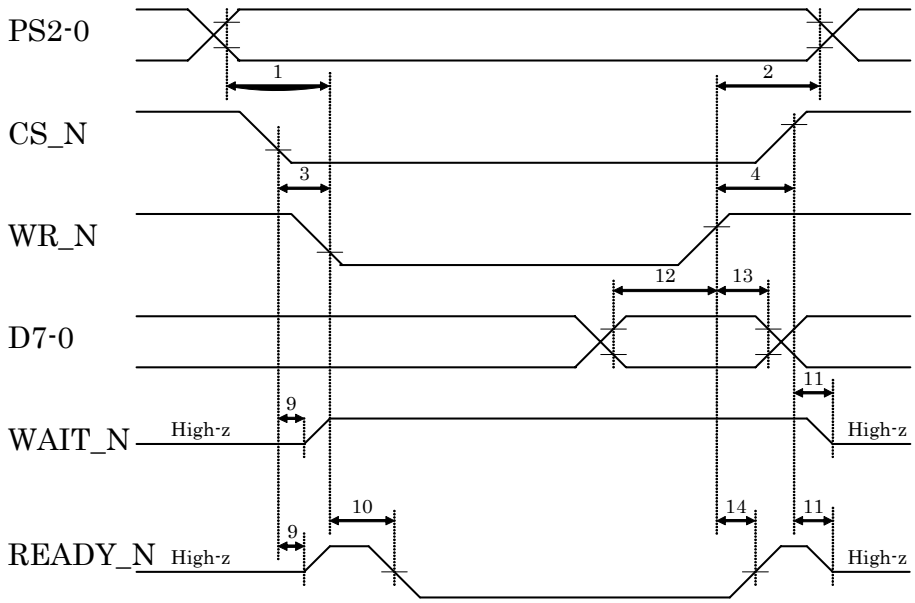
Note 2) Conditions to be WR_N and RD_N control. If not satisfying the specifications, they turn to CS_N control.

Note 3) “Command pulse” means a low active pulse when OR operation is performed between the CS_N signal and each of the WR_N and RD_N signals.

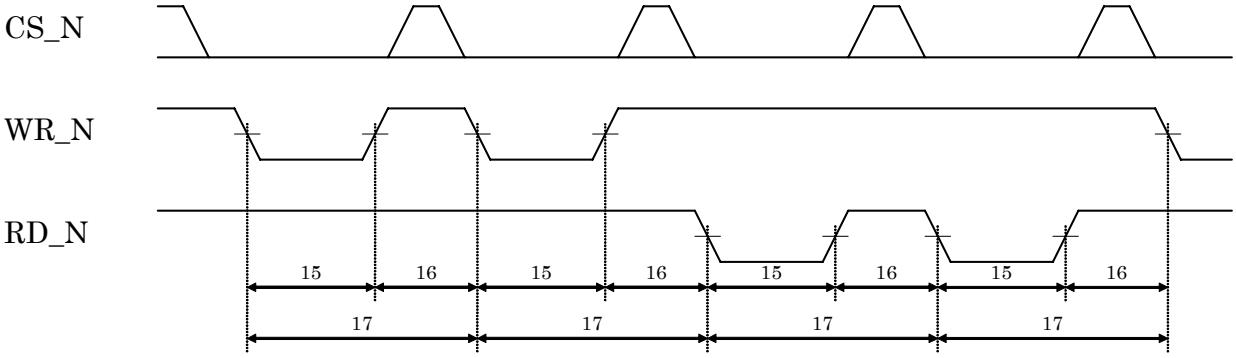
- CPU Read Cycle



- CPU Write Cycle



- Access Cycle

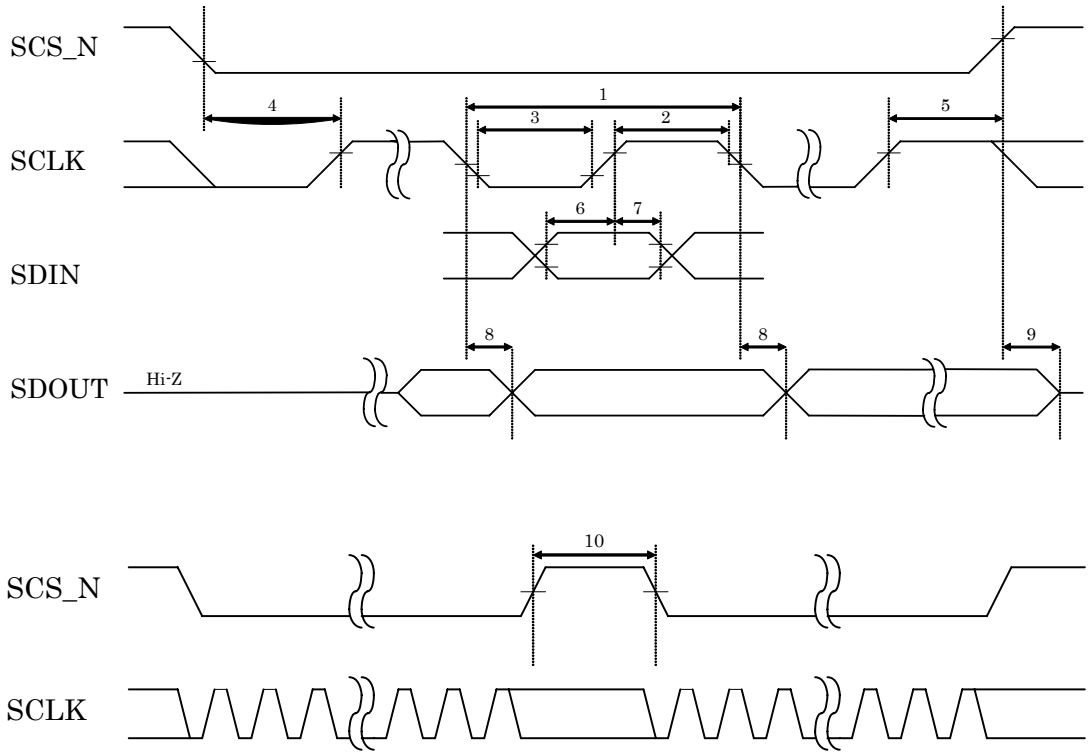


・Serial Interface

No.	Items	Symbol	Min.	Typ.	Max.	Unit	Note
1	SCLK Clock Cycle Time	t_{wSCLK}	400			ns	1
2	SCLK Clock High Level Pulse Width	t_{whSCLK}	200				1
3	SCLK Clock Low Level Pulse Width	t_{wlSCLK}	200				1
4	SCS_N: Setup Time	t_{sSCS}	50				
5	SCS_N: Hold Time	t_{hSCS}	50				
6	SDIN: Setup Time	t_{sSDI}	50				
7	SDIN: Hold Time	t_{hSDI}	50				
8	SDOUT: Output Data Delay Time	t_{dSDO}			100		2
9	SDOUT: Turn Off Time	$t_{offlSDO}$			20		
10	SCS_N: Pulse Inhibit Time	t_{iSCS}			400		

Note 1) In the initialization, the minimum value of t_{wSCLK} becomes XIN cycle×8 (t_{XIN} × 8), and minimum values of t_{whSCLK} and t_{wlSCLK} become XIN cycle×4 (t_{XIN} × 4).
Compare it with the value defined in the above table and use the larger value.

Note 2) In the initialization, the maximum value of t_{dSDO} becomes XIN cycle × 6＋100ns (t_{XIN} × 6 + 100ns).

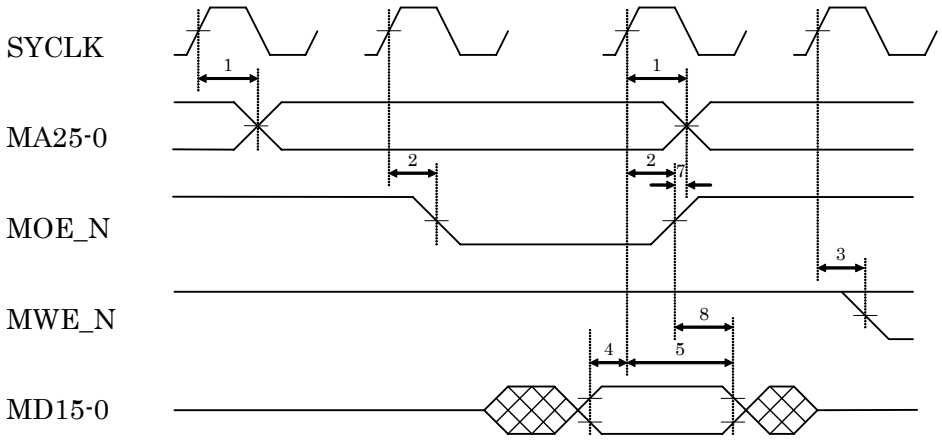


・Pattern Memory Interface

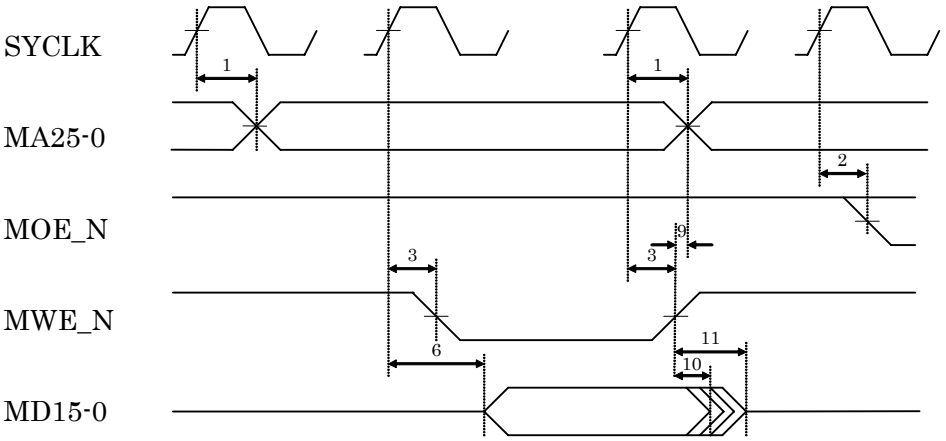
No.	Items	Symbol	Min.	Typ.	Max.	Unit	Note
1	MA25-0: Output Delay Time from SYCLK	t_{dMA}			14	ns	1
2	MOE_N: Output Delay Time from SYCLK	t_{dOE}	2		14		1
3	MWE_N: Output Delay Time from SYCLK	t_{dWE}	2		14		1
4	MD15-0: Input Setup Time to SYCLK	t_{sMD}	4				1
5	MD15-0: Input Hold Time from SYCLK	t_{hMD}	0				1
6	MD15-0: Output Delay Time from SYCLK	t_{dMD}			24		1
7	MA25-0: Hold Time from MOE_N	t_{hMAR}	0				
8	MD15-0: Input Hold Time from MOE_N, MA25-0	t_{hMDI}	0				
9	MA25-0: Hold Time from MWE_N	t_{hMAW}	0				
10	MD15-0: Hold Time from MWE_N	t_{hMDO}	1				
11	MD15-0: Turn Off Time from MWE_N	t_{offMDO}	1		10		
12	Output Turn Off/On Time from RAHZ_N	$t_{on/offRA}$			25		

Note 1) SYCLK is the internal clock.

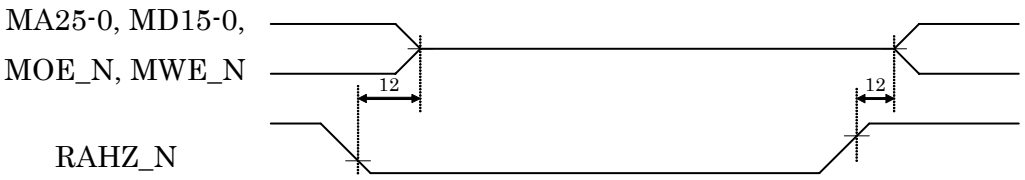
- Memory Access Cycle (Random Read Cycle)



- Memory Access Cycle (Write Cycle)



- RAHZ_N

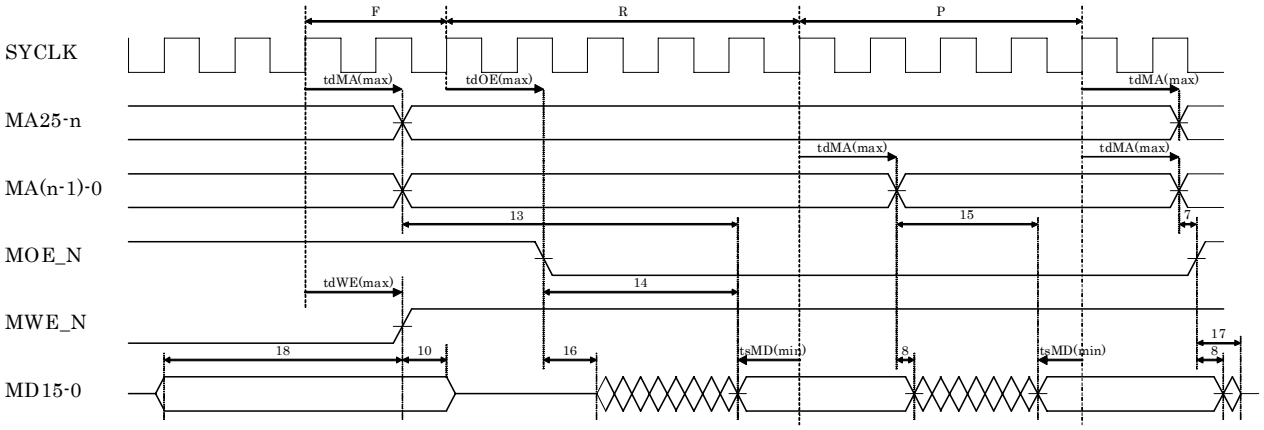


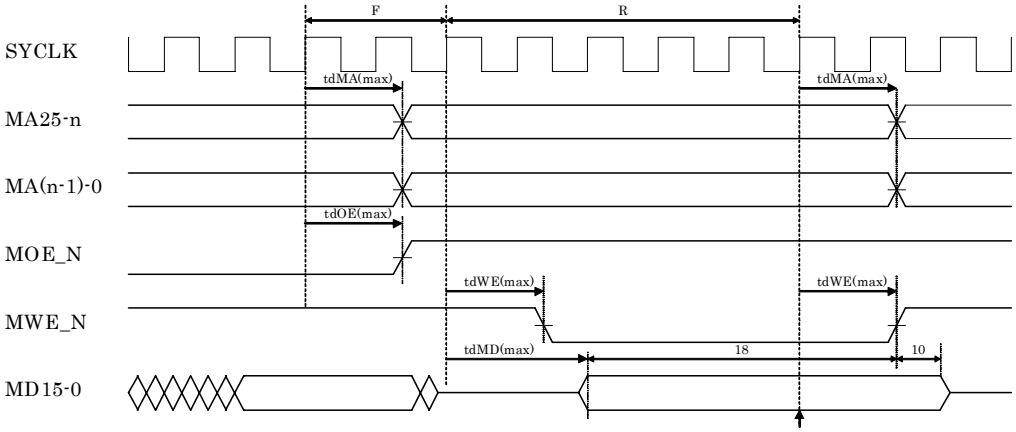
The AC characteristics of an external memory connecting to YGV632 must meet the following conditions.
(The following conditions are the values converted from the AC characteristics of the YGV632 pattern memory; they do not guarantee the following specifications directly. In addition, the following item names listed are those mainly for externally connected memory.)

"F", "R", and "P" in the below are as follows:

F= (R#2:FLTIM[1:0]+1) Number of Floating Clocks
R= (R#3:RDM[3:0]+1) Number of Random Access Clocks
P= (R#3:PAG[2:0]+1) Number of Page Mode Access Clock

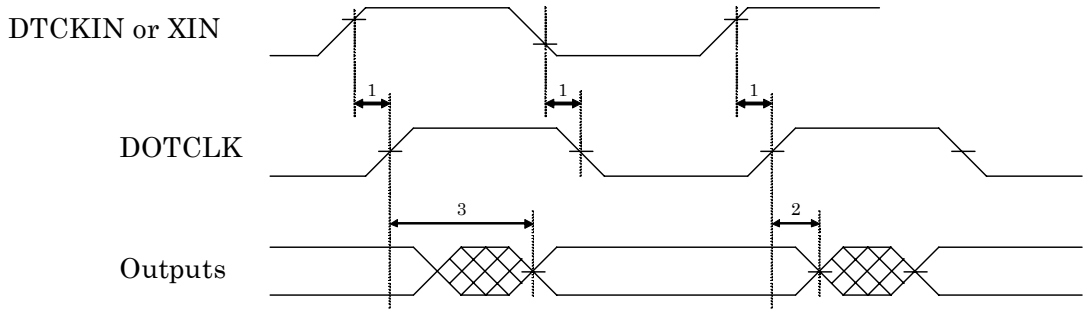
No.	Items	Conditions
13	Address, Access Time	It should be $(F + R) \times t_{SYCLK} - t_{dMA}(max) - t_{sMD}(min)$ or lower.
14	Output Enable Time	It should be $R \times t_{SYCLK} - t_{dOE}(max) - t_{sMD}(min)$ or lower.
15	Page Mode Access Time	It should be $P \times t_{SYCLK} - t_{dMA}(max) - t_{sMD}(min)$ or lower.
16	Data Turn On Time	It should be 0[ns] or over
17	Data Turn Off Time	It should be $F \times t_{SYCLK} - t_{dOE}(max) + t_{dWE}(min)$ or lower.
18	Data Setup Time	It should be $R \times t_{SYCLK} - t_{dMD}(max) + t_{dWE}(min)$ or lower.





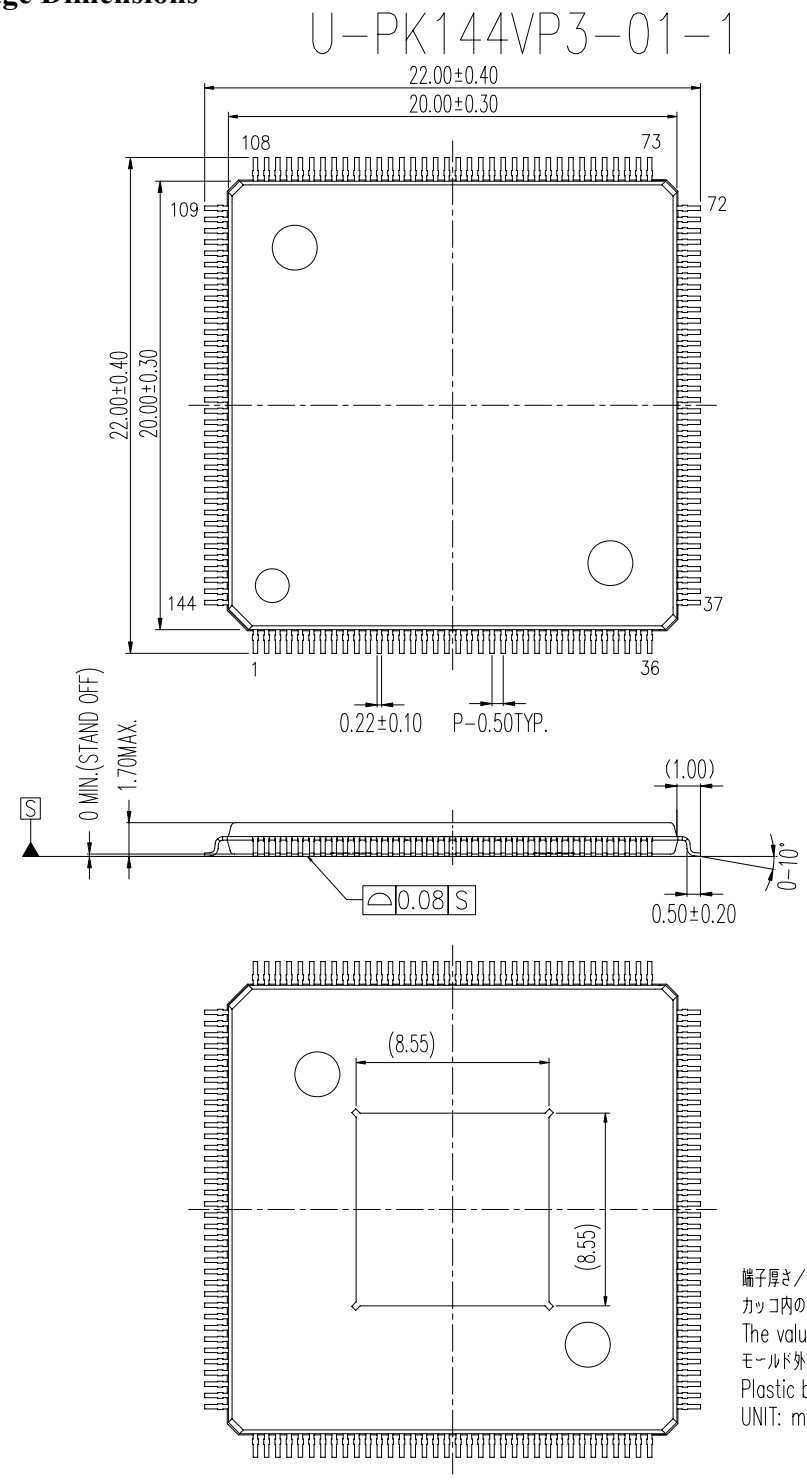
・Display Timing Signals

No.	Items	Symbol	Min.	Typ.	Max.	Unit	Note
1	DOTCLK: Delay Time	t_{dDOTC}			26	ns	
2	VSYNC_N, HCSYNC_N, BLANK_N, DR5-0, DG5-0, DB5-0: Output Hold Time	t_{hDISP}	0			ns	
3	VSYNC_N, HCSYNC_N, BLANK_N, DR5-0, DG5-0, DB5-0: Output Delay Time	t_{dDISP}			10	ns	



Note) the above figure shows the state that DOTCLK is not inverted.

■Package Dimensions



端子厚さ/Lead Thickness: 0.17±0.05
カッコ内の寸法値は参考値とする。
The value parenthesized is not specified.
モールド外形寸法はバリを含まない。
Plastic body dimensions do not include burr of resin.
UNIT: mm

注） 1. 表面実装LSIは、保管条件、および、半田付けについての特別な配慮が必要です。
2. 組立工場により、寸法や形状などが異なる場合があります。
詳しくはヤマハ代理店までお問い合わせください。

Note: 1. Special attention needs to be paid to the storage conditions and soldering method of the surface mount IC.
2. Dimension, form, etc. may differ depending on assembly plants.
For details, please contact your local Yamaha agent.

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PRECAUTIONS AND INSTRUCTIONS FOR SAFETY

	WARNING
Prohibited	Do not use the device under stresses beyond those listed in Absolute Maximum Ratings. Such stresses may become causes of breakdown, damages, or deterioration, causing explosion or ignition, and this may lead to fire or personal injury.
Prohibited	Do not mount the device reversely or improperly and also do not connect a supply voltage in wrong polarity. Otherwise, this may cause current and/or power-consumption to exceed the absolute maximum ratings, causing personal injury due to explosion or ignition as well as causing breakdown, damages, or deterioration. And, do not use the device again that has been improperly mounted and powered once.
Prohibited	Do not short between pins. In particular, when different power supply pins, such as between high-voltage and low-voltage pins, are shorted, smoke, fire, or explosion may take place.
Instructions	As to devices capable of generating sound from its speaker outputs, please design with safety of your products and system in mind, such as the consequences of unusual speaker output due to a malfunction or failure. A speaker dissipates heat in a voice-coil by air flow accompanying vibration of a diaphragm. When a DC signal (several Hz or less) is input due to device failure, heat dissipation characteristics degrade rapidly, thereby leading to voice-coil burnout, smoking or ignition of the speaker even if it is used within the rated input value.

	CAUTION
Prohibited	Do not use Yamaha products in close proximity to burning materials, combustible substances, or inflammable materials, in order to prevent the spread of the fire caused by Yamaha products, and to prevent the smoke or fire of Yamaha products due to peripheral components.
Instructions	Generally, semiconductor products may malfunction and break down due to aging, degradation, etc. It is the responsibility of the designer to take actions such as safety design of products and the entire system and also fail-safe design according to applications, so as not to cause property damage and/or bodily injury due to malfunction and/or failure of semiconductor products.
Instructions	The built-in DSP may output the maximum amplitude waveform suddenly due to malfunction from disturbances etc. and this may cause damage to headphones, external amplifiers, and human body (the ear). Please pay attention to safety measures for device malfunction and failure both in product and system design.
Instructions	As semiconductor devices are not nonflammable, overcurrent or failure may cause smoke or fire. Therefore, products should be designed with safety in mind such as using overcurrent protection circuits to control the amount of current during operation and to shut off on failure.
Instructions	Products should be designed with fail safe in mind in case of malfunction of the built-in protection circuits. Note that the built-in protection circuits such as overcurrent protection circuit and high-temperature protection circuit do not always protect the internal circuits. In some cases, depending on usage or situations, such protection circuit may not work properly or the device itself may break down before the protection circuit kicks in.
Instructions	Use a robust power supply. The use of an unrobust power supply may lead to malfunctions of the protection circuit, causing device breakdown, personal injury due to explosion, or smoke or fire.
Instructions	Product's housing should be designed with the considerations of short-circuiting between pins of the mounted device due to foreign conductive substances (such as metal pins etc.). Moreover, the housing should be designed with spatter prevention etc. due to explosion or burning. Otherwise, the spattered substance may cause bodily injury.
Instructions	The device may be heated to a high temperature due to internal heat generation during operation. Therefore, please take care not to touch an operating device directly.

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AGENT

YAMAHA CORPORATION

Address Inquiries to :
Semiconductor Sales & Marketing Department

■Head Office 203, Matsunokijima, Iwata,
Shizuoka, 438-0192, Japan
Tel. +81-539-62-4918 Fax.+81-539-62-5054

■Tokyo Office 2-17-11, Takanawa, Minato-ku,
Tokyo, 108-8586, Japan
Tel. +81-3-5488-5431 Fax.+81-3-5488-5088

■Osaka Office Universal City Wako Bldg.
6-2-82, Shimaya, Konohana-ku,
Osaka, 554-0024, Japan
Tel. +81-6-6465-0325 Fax.+81-6-6465-0391

Printed in Japan